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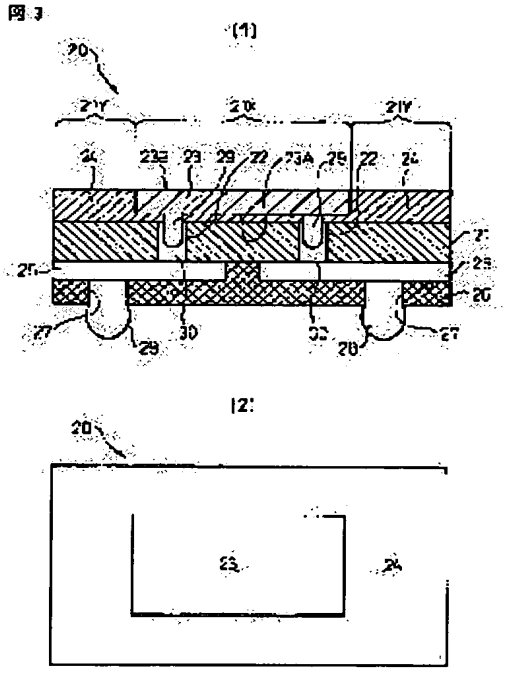
(54) SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a semiconductor device as a thin-type semiconductor package and its manufacturing method, by which the mounting height is reduced and is made constant at the same time, the production yield can be improved without complicated steps for mounting individual chips, the height of the semiconductor device can be made constant without being affected by a variance of chip thickness, and electric testings can be conducted at the same time.
SOLUTION: In this semiconductor device, a semiconductor element exposing its rear surface upward is mounted to the upper surface of an insulative tape base material having through holes in the thickness direction, and the sides of the semiconductor element are sealed with a sealing resin layer, and then the bottom parts of the through holes of the tape base material are formed by a metallic wiring formed under the tape base material. A solder resist layer having through holes in the thickness direction covers the lower surfaces of the metallic wiring and tape base material, and a connection terminal extending downward from the active surface of the semiconductor element is inserted into the through hole of the tape base material. Furtheremore, a filler made of conductive material is applied into a clearance between the connection terminal and the through hole of the tape base material, thereby connecting electrically the connection terminal with the metallic wiring.



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CLAIMS

[Claim(s)]
[Claim 1] The following member : on the top face of the insulating tape base material which has the through tube of the thickness direction, and this tape base material The semiconductor device carried by exposing a tooth back up and turning an active side caudad, It is formed in said tape base material top faces other than the field in which this semiconductor device was carried. The closure resin layer which closes the perimeter of a side face of this semiconductor device, metal wiring which is formed in the inferior surface of tongue of said tape base material, and takes up the lower limit of the through tube of this tape base material, and demarcates a pars basilaris ossis occipitalis, The solder resist layer which covers the inferior surface of tongue of this metal wiring and said tape base material, and has the through tube of the thickness direction, The external connection terminal which upheaved from the inferior surface of tongue of said metal wiring, was filled up with the through tube of said solder resist layer, penetrated, and was projected caudad, The connection terminal which was caudad prolonged from the active side of said semiconductor device, and was inserted into the through tube of said tape base material, And the semiconductor device characterized by including the filler which consists of the conductive ingredient which is filled up with the gap of this connection terminal and the wall of the through tube of said tape base material, and connects this connection terminal and said metal wiring electrically.
[Claim 2] The semiconductor device according to claim 1 with which said filler is characterized by being formed using a low-melt point point metal or a conductive paste.
[Claim 3] the conductor which penetrated said tape base material of the field in which said closure resin layer and this closure resin layer are formed, upper limit exposed to the top face of this closure resin layer, and the lower limit has connected to said metal wiring layer electrically -- the semiconductor device according to claim 1 or 2 characterized by including a column further.

[Claim 4] The insulating frame which replaces with said closure resin layer, is joined to said tape base material top faces other than the field in which said semiconductor device was carried, and encloses the side face of this semiconductor device through a gap, The closure resin layer which is filled up with the inside of this gap and closes the perimeter of a side face of this semiconductor device is included. the conductor which penetrated said tape base material of the field where this frame and this frame are joined, upper limit exposed to the top face of this frame, and the lower limit has connected to said metal wiring layer electrically -- the semiconductor device according to claim 1 characterized by including a column further.
[Claim 5] A semiconductor device given [from the active side of said semiconductor device to claims 1-4 characterized by the connection terminal prolonged caudad being the bump who consists of gold or copper] in any 1 term.
[Claim 6] The semiconductor device given [to claims 1-5] in any 1 term with which the external connection terminal which is filled up with opening of said solder resist layer, and is penetrated is characterized by being arranged with the gestalt of peripheral ones or an area array.
[Claim 7] A semiconductor device given [to claims 1-6 characterized by the thing of this through tube which it fills up with said filler to the location of upper limit mostly in the gap of said connection terminal and wall of the through tube of said tape base material] in any 1 term.
[Claim 8] A semiconductor device given [to claims 1-7 characterized by the top face of said closure resin layer and the tooth back of said semiconductor device having constituted the same flat surface] in any 1 term.
[Claim 9] a semiconductor device according to claim 3 or 4 carries out a laminating to two or more layers -- having -- the semiconductor devices of each class -- said conductor -- the component laminating mold semiconductor device characterized by connecting mutually electrically in the upper limit of a column, and the lower limit of said external connection terminal.
[Claim 10] It is the manufacture approach of a semiconductor device given [to claims 1-8] in any 1 term. Have the area which may include two or more semiconductor package units, and said through tube of the thickness direction is respectively formed in said tape base material and this solder resist layer which equipped the inferior surface of tongue with said metal wiring layer and said solder resist layer. Fill up said conductive ingredient into the through tube of this tape base material with the amount imperfectly filled up with this through tube, and said connection terminal of said semiconductor device of the need [of constituting two or more semiconductor package units] number is respectively inserted in the through tube to which the above-mentioned tape base material corresponds. the gap of this connection terminal and the wall of this through tube -- this through tube, while making it mostly filled up with this conductive ingredient to upper limit The closure resin layer which covers the top face of these tape base materials other than the field in which this semiconductor device was joined and carried in the top face of this tape base material, and this semiconductor device was carried, and closes the perimeter of a side face of this semiconductor device at least is formed. Then, the manufacture approach of the semiconductor device characterized for a part for the tooth-back flank of the upper part of this closure resin layer, and this semiconductor device by grinding and grinding, considering as predetermined thickness, carving this tape base material and subsequently to said semiconductor package unit considering as each semiconductor device.
[Claim 11] the time of being an approach according to claim 10 for manufacturing a semiconductor device according to claim 3, and forming a through tube in said tape base material -- a conductor according to claim 3 -- before forming another through tube which penetrates this tape base material in the location corresponding to a column and forming said closure resin layer -- this -- it was filled up with another through tube, and it projected from the top face of this tape base material -- this -- a conductor -- the manufacture approach of the semiconductor device characterized by to form a column.
[Claim 12] It is an approach according to claim 10 for manufacturing a semiconductor device according to claim 4. The insulating base material which prepared opening which specifies the wall of a frame according to claim 4 is joined to the top face of said tape base material. Another through tube which penetrates this insulating base material and this tape base material in the

location corresponding to a column is formed. the time of forming said through tube in this tape base material -- a conductor according to claim 4 -- before carrying said semiconductor device -- this -- it is filled up with another through tube, and exposes to the top face of this insulating base material -- this -- a conductor -- the manufacture approach of the semiconductor device characterized by forming a column, and forming said closure resin layer in a gap according to claim 4 after carrying this semiconductor device.
[Claim 13] The manufacture approach of a semiconductor device given [to claims 10-12 characterized by performing an electric trial before said grinding and polish or to the back after forming said closure resin layer] in any 1 term.
[Claim 14] The manufacture approach of a semiconductor device given [to claims 10-13] in any 1 term that the tape base material which may include said two or more semiconductor package units is characterized by having the shape of a with a 2 inches or more diameter [12 inch or less] disk.
[Claim 15] On the top face of the insulating tape base material which has metal wiring on the following member ** - **:** top face, and ** this tape base material It is the semiconductor device carried by exposing a tooth back up and turning an active side caudad. The semiconductor device which the lower limit of the connection terminal which projected from this active side to the lower part has connected to the top face of this metal wiring, ** The closure resin layer which is formed in the top face of this tape base material, and closes the perimeter of a side face of this semiconductor device, and is filled up with the gap of this active side of this semiconductor device, and the top face of this tape base material, and ** following -- (A) and (B) -- at least -- on the other hand -- : -- the conductor which was prolonged in the upper part from the top face of (A) this metal wiring, and penetrated the closure resin layer around [side face] this semiconductor device, and upper limit exposed up -- a column -- And the semiconductor device characterized by including the external connection terminal which was caudad prolonged from the inferior surface of tongue of (B) this metal wiring, penetrated this tape base material, and was projected caudad.
[Claim 16] The semiconductor device according to claim 15 characterized by the top face of said closure resin layer and the tooth back of said semiconductor device having constituted the same flat surface.
[Claim 17] It is the manufacture approach of the semiconductor device [equipped with the column] according to claim 15. as said member ** -- (A) -- a conductor -- Have the area which may include two or more semiconductor package units, and the tape base material which equipped the top face with said metal wiring is prepared. By joining said connection terminal of said active side of said semiconductor device of the need [of constituting two or more semiconductor package units] number to the top face of the above-mentioned metal wiring of the above-mentioned tape base material A column is formed. the conductor which carried this semiconductor device in the top face of this tape base material, and the lower limit joined to the top face of this metal wiring -- The closure resin layer which closes the perimeters of a side face of this semiconductor device including a column, and is filled up with the gap of this active side of this semiconductor device and the top face of this tape base material is formed. this metal wiring -- and -- this -- a conductor -- The upper limit of a column is exposed up. a part for then, the tooth-back flank of the upper part of this closure resin layer, and this semiconductor device -- grinding -- and -- while grinding and considering as predetermined thickness -- this -- a conductor -- subsequently The manufacture approach of the semiconductor device characterized by carving this tape base material into said semiconductor package unit, and considering as each semiconductor device.
[Claim 18] It is the manufacture approach of the semiconductor device according to claim 15 equipped with (B) external connection terminal as said member **. Have the area which may include two or more semiconductor package units, and a top face is equipped with said metal wiring. Have the through tube of the thickness direction in the location corresponding to said external connection terminal, and the tape base material with which the inferior surface of tongue of this metal wiring has demarcated the upper limit of this through tube is prepared. By joining said connection terminal of said active side of said semiconductor device of the need [of

constituting two or more semiconductor package units] number to the top face of the above-mentioned metal wiring of the above-mentioned tape base material The closure resin layer which carries this semiconductor device in the top face of this tape base material, and closes the perimeters of a side face of this semiconductor device including this metal wiring, and is filled up with the gap of this active side of this semiconductor device and the top face of this tape base material is formed. It carries out to the following process (S1) and (S2) this order, or a reverse order. A part for the tooth-back flank of the upper part of :(S1) this closure resin layer, and this semiconductor device Then, grinding and the process which is ground and is made into predetermined thickness, and (S2) the process which forms the external connection terminal which was caudad prolonged from the inferior surface of tongue of the above-mentioned metal wiring which demarcates the upper limit of the above-mentioned through tube, was filled up with this through tube, and was projected caudad -- subsequently The manufacture approach of the semiconductor device characterized by carving this tape base material into said semiconductor package unit, and considering as each semiconductor device.

[Claim 19] It is the manufacture approach of the semiconductor device [equipped with the column and (B) external connection terminal] according to claim 15. as said member ** -- (A) -- a conductor -- Have the area which may include two or more semiconductor package units, and a top face is equipped with said metal wiring. Have the through tube of the thickness direction in the location corresponding to said external connection terminal, and the tape base material with which the inferior surface of tongue of this metal wiring has demarcated the upper limit of this through tube is prepared. By joining said connection terminal of said active side of said semiconductor device of the need [of constituting two or more semiconductor package units] number to the top face of the above-mentioned metal wiring of the above-mentioned tape base material A column is formed. the conductor which carried this semiconductor device in the top face of this tape base material, and the lower limit joined to the top face of this metal wiring -- The closure resin layer which closes the perimeters of a side face of this semiconductor device including a column, and is filled up with the gap of this active side of this semiconductor device and the top face of this tape base material is formed. this metal wiring -- and -- this -- a conductor -- Then, while it carries out to the following process (S1) and (S2) this order, or a reverse order, and grinding and making a part for the tooth-back flank of the upper part of :(S1) this closure resin layer, and this semiconductor device into grinding and the thickness which is predetermined said conductor -- the process at which the upper limit of a column is exposed up, and (S2) the process which forms the external connection terminal which was caudad prolonged from the inferior surface of tongue of the above-mentioned metal wiring which demarcates the upper limit of the above-mentioned through tube, was filled up with this through tube, and was projected caudad -- subsequently The manufacture approach of the semiconductor device characterized by carving this tape base material into said semiconductor package unit, and considering as each semiconductor device.

[Claim 20] The following member: The semiconductor device which the closure is carried out to the interior of the resin object of predetermined thickness, and this resin object, and is characterized by to include the connection terminal which exposed the tooth back to the top face of this resin object, was caudad prolonged from the active side of metal wiring formed in the inferior surface of tongue of the semiconductor device which turned the active side caudad, and this resin object, and this semiconductor device, and the lower limit has connected to the top face of this metal wiring.

[Claim 21] The semiconductor device according to claim 20 characterized by the top face of said resin object and the tooth back of said semiconductor device having constituted the same flat surface.

[Claim 22] The semiconductor device according to claim 20 or 21 characterized by including further the connection bump who was formed in the wrap solder resist layer and the inferior surface of tongue of this metal wiring in the whole inferior surface of tongue of said resin object, penetrated the above-mentioned solder resist layer including said metal wiring, and has projected caudad.

[Claim 23] two or more conductors which penetrated said resin object from the top face of said

metal wiring, and were prolonged up, and upper limit has exposed to the top face of this resin object -- a semiconductor device given [to claims 20-22 characterized by including a column further] in any 1 term.
[Claim 24] said conductor -- the semiconductor device according to claim 23 characterized by the side face of a column being exposed to the side face of said resin object.
[Claim 25] A semiconductor device given [to claims 20-24 characterized by including further the capacitor which the closure is carried out to the interior of said resin object, and is carrying out direct continuation to this metal wiring] in any 1 term.
[Claim 26] The semiconductor device according to claim 25 with which said capacitor is an opposite monotonous mold, and the plate surface of each plate is characterized by the parallel thing to the thickness direction of said resin object.
[Claim 27] said resin -- a semiconductor device given [to claims 20-26 characterized by the inorganic filler distributing inside of the body] in any 1 term.
[Claim 28] a semiconductor device according to claim 23 carries out a laminating to two or more layers -- having -- the semiconductor devices of each class -- said conductor -- the component laminating mold semiconductor device characterized by connecting mutually electrically through a connection bump on the upper limit of a column, and the inferior surface of tongue of said metal wiring.
[Claim 29] the conductor which the semiconductor devices which the semiconductor device according to claim 24 is mutually connected on the side face, and adjoin the side exposed to the side face of said resin object -- the component parallel connected type semiconductor device characterized by connecting mutually electrically on the side faces of a column.
[Claim 30] The laminating of the semiconductor device according to claim 24 is carried out to two or more layers, and it connects mutually on the side face. It connects mutually electrically through the connection bump on the upper limit of a column, and the inferior surface of tongue of said metal wiring. the semiconductor devices of each class -- said conductor -- and the conductor which the semiconductor devices which adjoin the side exposed to the side face of said resin object -- the component laminating parallel connected type semiconductor device characterized by connecting mutually electrically on the side faces of a column.
[Claim 31] It is the manufacture approach of a semiconductor device given [to claims 20-25] in any 1 term. By turning the active side of said semiconductor device to the top face of the metal substrate which has the area which may include two or more semiconductor package units caudad, and joining the tip of said connection terminal to it By carrying this semiconductor device in this metal substrate, and covering the whole top face of this metal substrate by resin The resin object with which the closure of this semiconductor device was carried out to the interior, and this metal substrate was joined to the inferior surface of tongue is formed. It carries out to the following process (S1) and (S2) this order, or a reverse order. A part for the tooth-back flank of the upper part of :(S1) this resin object, and this semiconductor device Then, grinding and the process which is ground and is made into predetermined thickness, and (S2) the process which forms in the inferior surface of tongue of the above-mentioned resin object metal wiring to which the top face was connected to the lower limit of this connection terminal by carrying out patterning of this metal substrate -- subsequently The manufacture approach of the semiconductor device characterized by carving this resin object into said semiconductor package unit, and considering as each semiconductor device.
[Claim 32] after carrying said semiconductor device in said metal substrate, before forming said resin object -- the top face of this metal substrate -- a conductor -- the manufacture approach of the semiconductor device according to claim 31 characterized by including further the process which forms a column.
[Claim 33] said conductor -- the manufacture approach of the semiconductor device according to claim 32 characterized by forming a column so that upper limit and/or a side face may be exposed from said resin object.
[Claim 34] It is the approach of manufacturing a semiconductor device given [to claims 20-25] in any 1 term. On the top face of the metal substrate which has the area which may include two or more semiconductor package units By turning the active side of said semiconductor device to

the top face of the above-mentioned circuit pattern of the process which produces the compound metal plate which prepared the circuit pattern which consists of a metal of a different kind, and the above-mentioned compound metal plate caudad, and joining the tip of said connection terminal to this metal substrate By carrying this semiconductor device in this compound metal plate, and covering the whole top face of this compound metal plate by resin The resin object with which the closure of this semiconductor device was carried out to the interior, and this compound metal plate was joined to the inferior surface of tongue is formed. It carries out by the following process (S1) and (S2) this order, or the reverse order. A part for the tooth-back flank of the upper part of :(S1) this resin object, and this semiconductor device Then, grinding and the process which is ground and is made into predetermined thickness, And (S2) by etching removing this metal substrate of this compound metal plate, and leaving this circuit pattern The manufacture approach of the process which forms in the inferior surface of tongue of the above-mentioned resin object metal wiring which consists of this circuit pattern by which the top face was connected to the lower limit of this connection terminal, and the semiconductor device characterized by carving this resin object and subsequently to said semiconductor package unit considering as each semiconductor device.
[Claim 35] after carrying said semiconductor device in said compound metal plate, before forming said resin object -- the top face of this metal substrate -- a conductor -- the manufacture approach of the semiconductor device according to claim 34 characterized by including further the process which forms a column.
[Claim 36] said conductor -- the manufacture approach of the semiconductor device according to claim 35 characterized by forming a column so that upper limit and/or a side face may be exposed from said resin object.
[Claim 37] The manufacture approach of the semiconductor device according to claim 31 or 34 characterized by including further the processes including this metal wiring which are formed in a wrap solder resist layer and the inferior surface of tongue of this metal wiring in the whole inferior surface of tongue of this resin object, and form the connection bump who penetrated the above-mentioned solder resist layer and has projected caudad after forming said metal wiring in the inferior surface of tongue of said resin object.

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* NOTICES *

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the semiconductor device and its manufacture approach as a thin package about a semiconductor device and its manufacture approach.
[0002]
[Description of the Prior Art] Conventionally, TCP (tape career package) for which the semiconductor device as a thin package which carried the semiconductor device (semiconductor chips, such as LSI) may be best adapted in thin-shape-izing and a miniaturization of the

formation of many pins, contraction of a connection terminal pitch, and the whole equipment has spread.
[0003] TCP carries a semiconductor device in an insulating tape-like base material (usually resin film) with a TAB (tape automation ITEDO bonding) method, and is manufactured. After sticking copper foil on the resin film which prepared opening of a predetermined pattern first typically, patterning of the copper foil is carried out by etching, and a predetermined copper lead is formed. Next, one semiconductor package unit is completed by positioning and holding a semiconductor device (semiconductor chip) in opening of a resin film, and carrying out the resin seal of a part of copper lead to a semiconductor chip, after joining two or more connection terminals (generally golden bump) of a chip, and two or more copper leads with which it corresponds on a resin film. And many semiconductor package units are formed on one film in a resin film by repeating the above-mentioned actuation for every opening with delivery intermittently. The semiconductor device as each semiconductor package is obtained by the last by carrying out cutting separation of each semiconductor package unit by which a large number formation was carried out along with the longitudinal direction of a film mutually.
[0004] Drawing 1 is the perspective view showing the conventional semiconductor device after connecting the lead of TCP with a semiconductor chip, and shows the condition before cutting each TCP from a tape. TCP10 uses the resin film (for example, polyimide resin film) 1 as a base material, and has the lead 2 formed by etching of copper foil on it. Moreover, the sprocket hole 3 has opened in the edges on both sides of the resin film 1 for the film advance. Furthermore, opening (generally called the "device hole") 5 and the window hole 9 for holding a semiconductor chip 4 so that it may be illustrated can also be opened in the center section of the resin film 1.
[0005] The condition of connection of the lead of a semiconductor chip and a package is shown in the sectional view of drawing 2 which expanded the core of the semiconductor device of drawing 1 . After positioning the semiconductor chip 4 in the device hole 5 of the resin film 1 and having been arranged, the tip of lead 2 is joined by the bump 6 on the electrode (projection which usually consists of gold plate). Junction of this lead is usually performed by package bonding using the bonding tool of dedication. In addition, in order to help junction with a bump 6, prior to a bonding process, gold plate etc. is beforehand performed at the tip of the lead 2 which consists of copper. Finally, although not shown in drawing 1 , in order to protect a semiconductor chip 4 and lead 6 from the humidity of a perimeter environment, contamination, etc., as both are wrapped in, it closes by resin 7. As resin 7 for the closures, an epoxy resin is used, for example.
[0006] However, there was a problem of following (a) - (e) in the above-mentioned conventional semiconductor device.
(a) Since a limitation is in reduction of the installation height of the semiconductor chip to a resin film, a limitation is in thin shape-ization of a semiconductor device. That is, immobilization of a semiconductor device needs the above thickness for a copper lead, the resin film used as the supporter material, and the whole equipment to some extent, in order to secure installation reinforcement, since it is made with the copper lead which projected long and slender in the shape of a beam to the opening circles of a resin film. Supposing it makes it reinforce with the resin seal section temporarily, the large range must be closed thickly, but if it is difficult to cross to the large range and to secure the integrity of the closure and closes thickly, it moves against thin shape-ization.
[0007] (b) required for thin-shape-izing of a semiconductor device -- thin -- weak -- curvature -- being easy -- the handling of a semiconductor chip, such as requiring a separately special carrier, is very complicated, and improvement not only in requiring many processes but the manufacture yield is also difficult for it.
(c) Since it is necessary to carry out alignment of each semiconductor chip to opening of a resin film one by one, and to join, a production process becomes complicated and long for manufacturing many semiconductor packages.
[0008] (d) Since the component laminating mold semiconductor device which carried out the laminating of the semiconductor chip to two or more layers needs to carry out alignment and bonding of each semiconductor chip to opening of a resin film and needs to attach it, it becomes still more complicated [a production process] and long.

(e) When dispersion in thickness is in each chip, since dispersion in height arises in a semiconductor device as a result of there being dispersion also in each installation height, it is difficult to carry out collectively, before carrying out cutting separation of the electric trial per semiconductor package.

[0009]

[Problem(s) to be Solved by the Invention] The problem of the above-mentioned conventional technique is solved, it equalizes at the same time it reduces installation height, and this invention does not need the complicated process for each chip installation, but improves the manufacture yield, the height of a semiconductor device is equalized, without being influenced by thickness dispersion of a chip, and it aims at offering the semiconductor device and its manufacture approach as a thin semiconductor package in which package activation of an electric trial is possible.

[0010]

[The means for solving a technical problem and the gestalt of implementation of invention] In order to attain the above-mentioned purpose, the semiconductor device of the 1st invention The following member : on the top face of the insulating tape base material which has the through tube of the thickness direction, and this tape base material The semiconductor device carried by exposing a tooth back up and turning an active side caudad, It is formed in said tape base material top faces other than the field in which this semiconductor device was carried. The closure resin layer which closes the perimeter of a side face of this semiconductor device, metal wiring which is formed in the inferior surface of tongue of said tape base material, and takes up the lower limit of the through tube of this tape base material, and demarcates a pars basilaris ossis occipitalis, The solder resist layer which covers the inferior surface of tongue of this metal wiring and said tape base material, and has the through tube of the thickness direction, The external connection terminal which upheaved from the inferior surface of tongue of said metal wiring, was filled up with the through tube of said solder resist layer, penetrated, and was projected caudad, The connection terminal which was caudad prolonged from the active side of said semiconductor device, and was inserted into the through tube of said tape base material, And it is filled up with the gap of this connection terminal and the wall of the through tube of said tape base material, and is characterized by including the filler which consists of the conductive ingredient which connects this connection terminal and this metal wiring electrically.

[0011] The approach of manufacturing the semiconductor device of the 1st invention of the above Have the area which may include two or more semiconductor package units, and said through tube of the thickness direction is respectively formed in said tape base material and this solder resist layer which equipped the inferior surface of tongue with said metal wiring layer and said solder resist layer. Fill up said conductive ingredient into the through tube of this tape base material with the amount imperfectly filled up with this through tube, and said connection terminal of said semiconductor device of the need [of constituting two or more semiconductor package units] number is respectively inserted in the through tube to which the above-mentioned tape base material corresponds. the gap of this connection terminal and the wall of this through tube -- this through tube, while making it mostly filled up with this conductive ingredient to upper limit The closure resin layer which covers the top face of these tape base materials other than the field in which this semiconductor device was joined and carried in the top face of this tape base material, and this semiconductor device was carried, and closes the perimeter of a side face of this semiconductor device at least is formed. Then, a part for the tooth-back flank of the upper part of this closure resin layer and this semiconductor device is characterized by grinding and grinding, considering as predetermined thickness, carving this tape base material and subsequently to said semiconductor package unit, considering as each semiconductor device.

[0012] The connection terminal which according to the 1st invention was caudad prolonged from the active side of a semiconductor device, and was inserted into the through tube of a tape base material, And by having been filled up with the gap of a connection terminal and the wall of the through tube of a tape base material, and having considered as the structure equipped with the filler which consists of the conductive ingredient which connects a connection terminal and

metal wiring electrically Since a semiconductor device is electrically connectable with a metal wiring layer with the filler which consists of the conductive ingredient filled up with the connection terminal and gap inserted in the through tube of a tape base material while a semiconductor device is joinable to a direct tape base material in respect of active Compared with the structure which fixes a semiconductor device with a lead in opening of a tape base material like the conventional technique, installation reinforcement can be secured easily and can be thin-shape-ized conventionally.
[0013] According to the 1st invention, further, where it fixed many semiconductor devices on the tape base material and the resin seal of the side face perimeter of a semiconductor device is carried out the tooth back and closure resin layer of a semiconductor device -- the grinding from a top -- and, since it grinds and height can be reduced to a predetermined value Can deal with each semiconductor chip in the thick condition, without making it thin, and it needs neither a complicated process nor a special carrier like before. Many semiconductor package units are put in block as one fixed to the tape base material, and can be manufactured. After being able to arrange the height of the semiconductor device as a semiconductor package with homogeneity thinly, also being able to perform an electric trial collectively, and shortening a production process and improving the product yield, it can thin-shape-ize conventionally.
[0014] The semiconductor device by one gestalt of the 1st invention penetrates said tape base material of the field in which the ** aforementioned closure resin layer and said closure resin layer are formed. the conductor which upper limit exposed to the top face of this closure resin layer, and the lower limit has connected to said metal wiring layer electrically -- in the structure which contains a column further Or the insulating frame which replaces with the ** aforementioned closure resin layer, is joined to said tape base material top faces other than the field in which said semiconductor device was carried, and encloses the side face of this semiconductor device through a gap, the conductor which penetrated this tape base material of a field to which this frame and this frame are joined including the closure resin layer which is filled up with the inside of this gap and closes the perimeter of a side face of this semiconductor device, upper limit exposed to the top face of this frame, and the lower limit has connected to said metal wiring layer electrically -- it is the structure which contains a column further.
[0015] Especially if the structure of the above-mentioned ** or ** is applied to manufacture of a laminating mold semiconductor device, it is advantageous. the semiconductor device of the above-mentioned ** or the above-mentioned ** carries out the laminating of the laminating mold semiconductor device of the 1st invention manufactured by this to two or more layers -- having -- the semiconductor devices of each class -- said conductor -- it is the structure connected mutually electrically in the upper limit of a column, and the lower limit of said external connection terminal. In the semiconductor device of the 1st invention, the connection terminal caudad prolonged from the active side of said semiconductor device consists of the bump of gold or copper typically.
[0016] In the semiconductor device of the 1st invention, the external connection terminal which is filled up with opening of said solder resist layer, and is penetrated is arranged with the gestalt of peripheral one or an area array according to the application of a semiconductor device, or a request of a customer. In the semiconductor device of the 1st invention, the thing of this through tube for which said filler is mostly filled up with the gap of said connection terminal and wall of the through tube of said tape base material to the location of upper limit is desirable. That is, the amount of a filler is set up so that the sum total volume with the connection terminal of a semiconductor device inserted later may become almost equal to the volume of the through tube (metal wiring demarcates a pars basilaris ossis occipitalis) of a tape base material. Thereby, connection between a connection terminal and metal wiring accomplishes certainly, and it is prevented that an excessive conductive ingredient is full of coincidence from through tube upper limit. As a conductive ingredient, a low-melt point point metal or a conductive paste can be used.

[0017] In the manufacture approach of the 1st invention, since the height of the semiconductor package unit of a large number formed on the tape base material is equal to homogeneity, after forming said closure resin layer, although it bundles up easily and an electric trial is performed

before said grinding and polish or to the back, it can do. The tape base material used for the manufacture approach of the 1st invention is the size which may include said two or more semiconductor package units, and it is desirable to have the shape of a disk from the diameter of 2 inches to 12 inches. Since a facility of the existing grinding machine, a cutting machine, etc. which process the semi-conductor wafer of the same size can be used by this, the costs for the part and a new facility can be reduced.

[0018] The insulating tape base material with which the semiconductor device of the 2nd invention has metal wiring on the following member ** - **:** top face, ** It is the semiconductor device carried in the top face of this tape base material by exposing a tooth back up and turning an active side caudad. The semiconductor device which the lower limit of the connection terminal which projected from this active side to the lower part has connected to the top face of this metal wiring, ** The closure resin layer which is formed in the top face of this tape base material, and closes the perimeter of a side face of this semiconductor device, and is filled up with the gap of this active side of this semiconductor device, and the top face of this tape base material, and ** following -- (A) and (B) -- at least -- on the other hand -- : -- the conductor which was prolonged in the upper part from the top face of (A) this metal wiring, and penetrated the closure resin layer around [side face] this semiconductor device, and upper limit exposed up -- a column -- And it is characterized by including the external connection terminal which was caudad prolonged from the inferior surface of tongue of (B) this metal wiring, and penetrated this tape base material, and the lower limit exposed caudad. Typically, the top face of said closure resin layer and the tooth back of said semiconductor device have constituted the same flat surface.

[0019] the manufacture approach of the semiconductor device the 2nd invention -- as member ** -- (A) -- a conductor -- the gestalt of following (1) - (3) is taken according to three cases equipped with both a column, and (B) external connection both [one side or].

(1) as member ** -- (A) -- a conductor -- the manufacture approach of the semiconductor device the 2nd invention equipped with the column Have the area which may include two or more semiconductor package units, and the tape base material which equipped the top face with said metal wiring is prepared. By joining said connection terminal of said active side of said semiconductor device of the need [of constituting two or more semiconductor package units] number to the top face of the above-mentioned metal wiring of the above-mentioned tape base material A column is formed. the conductor which carried this semiconductor device in the top face of this tape base material, and the lower limit joined to the top face of this metal wiring -- The closure resin layer which closes the perimeters of a side face of this semiconductor device including a column, and is filled up with the gap of this active side of this semiconductor device and the top face of this tape base material is formed. this metal wiring -- and -- this -- a conductor -- a part for then, the tooth-back flank of the upper part of this closure resin layer, and this semiconductor device -- grinding -- and -- while grinding and considering as predetermined thickness -- this -- a conductor -- it is characterized by exposing the upper limit of a column up, carving this tape base material subsequently to said semiconductor package unit, and considering as each semiconductor device.

[0020] (2) The manufacture approach of the semiconductor device the 2nd invention equipped with (B) external connection terminal as member ** Have the area which may include two or more semiconductor package units, and a top face is equipped with said metal wiring. Have the through tube of the thickness direction in the location corresponding to said external connection terminal, and the tape base material with which the inferior surface of tongue of this metal wiring has demarcated the upper limit of this through tube is prepared. By joining said connection terminal of said active side of said semiconductor device of the need [of constituting two or more semiconductor package units] number to the top face of the above-mentioned metal wiring of the above-mentioned tape base material The closure resin layer which carries this semiconductor device in the top face of this tape base material, and closes the perimeters of a side face of this semiconductor device including this metal wiring, and is filled up with the gap of this active side of this semiconductor device and the top face of this tape base material is formed. It carries out to the following process (S1) and (S2) this order, or a reverse order. A part

for the tooth-back flank of the upper part of :(S1) this closure resin layer, and this semiconductor device Then, grinding and the process which is ground and is made into predetermined thickness, And (S2) it is characterized by the process which forms the external connection terminal which was caudad prolonged from the inferior surface of tongue of the above-mentioned metal wiring which demarcates the upper limit of the above-mentioned through tube, was filled up with this through tube, and exposed the lower limit caudad, and carving this tape base material and subsequently to said semiconductor package unit, considering as each semiconductor device.

[0021] (3) as member ** -- (A) -- a conductor -- the manufacture approach of the semiconductor device the 2nd invention equipped with the column and (B) external connection terminal Have the area which may include two or more semiconductor package units, and a top face is equipped with said metal wiring. Have the through tube of the thickness direction in the location corresponding to said external connection terminal, and the tape base material with which the inferior surface of tongue of this metal wiring has demarcated the upper limit of this through tube is prepared. By joining said connection terminal of said active side of said semiconductor device of the need [of constituting two or more semiconductor package units] number to the top face of the above-mentioned metal wiring of the above-mentioned tape base material A column is formed. the conductor which carried this semiconductor device in the top face of this tape base material, and the lower limit joined to the top face of this metal wiring -- The closure resin layer which closes the perimeters of a side face of this semiconductor device including a column, and is filled up with the gap of this active side of this semiconductor device and the top face of this tape base material is formed. this metal wiring -- and -- this -- a conductor -- It carries out to the following process (S1) and (S2) this order, or a reverse order. A part for the tooth-back flank of the upper part of :(S1) this closure resin layer, and this semiconductor device Then, grinding and the process which is ground and is made into predetermined thickness, And (S2) it is characterized by the process which forms the external connection terminal which was caudad prolonged from the inferior surface of tongue of the above-mentioned metal wiring which demarcates the upper limit of the above-mentioned through tube, was filled up with this through tube, and exposed the lower limit caudad, and carving this tape base material and subsequently to said semiconductor package unit, considering as each semiconductor device.

[0022] Since according to the 2nd invention it can consider as still briefer structure rather than a connection terminal and metal wiring connect through a filler within the through tube of a tape base material like the 1st invention, when the lower limit of the connection terminal which projected from the active side of a semiconductor device caudad considered as the structure connected to the top face of metal wiring on a tape base material top face, the productivity of a thin semiconductor device can be raised further.

[0023] Where it fixed many semiconductor devices on the tape base material and the resin seal of the side face perimeter of a semiconductor device is carried out like the 1st invention also in the 2nd invention the tooth back and closure resin layer of a semiconductor device -- the grinding from a top -- and, since it grinds and height can be reduced to a predetermined value Can deal with each semiconductor chip in the thick condition, without making it thin, and it needs neither a complicated process nor a special carrier like before. Many semiconductor package units are put in block as one fixed to the tape base material, and can be manufactured. After being able to arrange the height of the semiconductor device as a semiconductor package with homogeneity thinly, also being able to perform an electric trial collectively, and shortening a production process and improving the product yield, it can thin-shape-ize conventionally.

[0024] The closure of the semiconductor device of the 3rd invention is carried out to the interior of the resin object of the following member:predetermined thickness, and this resin object, and it exposes a tooth back to the top face of this resin object, and is characterized by to be included metal wiring formed in the inferior surface of tongue of the semiconductor device which turned the active side caudad, and this resin object, and the connection terminal which was caudad prolonged from the active side of this semiconductor device, and the lower limit has connected to the top face of this metal wiring. Typically, the top face of said resin object and the tooth

back of said semiconductor device have constituted the same flat surface.
[0025] The 1st method of manufacturing the semiconductor device of the 3rd invention By turning the active side of said semiconductor device to the top face of the metal substrate which has the area which may include two or more semiconductor package units caudad, and joining the tip of said connection terminal to it By carrying this semiconductor device in this metal substrate, and covering the whole top face of this metal substrate by resin The resin object with which the closure of this semiconductor device was carried out to the interior, and this metal substrate was joined to the inferior surface of tongue is formed. It carries out to the following process (S1) and (S2) this order, or a reverse order. A part for the tooth-back flank of the upper part of :(S1) this resin object, and this semiconductor device Then, grinding and the process which is ground and is made into predetermined thickness, And (S2) by carrying out patterning of this metal substrate, a top face is characterized by the process which forms in the inferior surface of tongue of the above-mentioned resin object metal wiring connected to the lower limit of this connection terminal, and carving this resin object and subsequently to said semiconductor package unit, considering as each semiconductor device.
[0026] The 2nd method of manufacturing the semiconductor device of the 3rd invention On the top face of the metal substrate which has the area which may include two or more semiconductor package units By turning the active side of said semiconductor device to the top face of the above-mentioned circuit pattern of the process which produces the compound metal plate which prepared the circuit pattern which consists of a metal of a different kind, and the above-mentioned compound metal plate caudad, and joining the tip of said connection terminal to this metal substrate By carrying this semiconductor device in this compound metal plate, and covering the whole top face of this compound metal plate by resin The resin object with which the closure of this semiconductor device was carried out to the interior, and this compound metal plate was joined to the inferior surface of tongue is formed. It carries out by the following process (S1) and (S2) this order, or the reverse order. A part for the tooth-back flank of the upper part of :(S1) this resin object, and this semiconductor device Then, grinding and the process which is ground and is made into predetermined thickness, And (S2) by etching removing this metal substrate of this compound metal plate, and leaving this circuit pattern A top face is characterized by the process which forms in the inferior surface of tongue of the above-mentioned resin object metal wiring which consists of this circuit pattern connected to the lower limit of this connection terminal, and carving this resin object and subsequently to said semiconductor package unit, considering as each semiconductor device.
[0027] While-izing can be carried out [thin shape] more nearly further than the 1st invention and the 2nd invention by having considered as the structure which does not contain a tape base material according to the 3rd invention, there are few members, and since it is briefer structure, still higher productivity can be attained. the 3rd invention -- also setting -- the resin of one -- the inside of the body -- many semiconductor devices -- closing -- the tooth back and resin object of a semiconductor device -- the grinding from a top -- and, since it grinds and height can be reduced to a predetermined value Can deal with each semiconductor chip in the thick condition, without making it thin, and it needs neither a complicated process nor a special carrier like before. It bundles up as one fixed to the inside of the body, and can manufacture. many semiconductor package units -- resin -- After being able to arrange the height of the semiconductor device as a semiconductor package with homogeneity thinly, also being able to perform an electric trial collectively, and shortening a production process and improving the product yield, it can thin-shape-ize conventionally.
[0028] In one desirable gestalt, the connection bump who was formed in the wrap solder resist layer and the inferior surface of tongue of this metal wiring in the whole inferior surface of tongue of said resin object, penetrated the above-mentioned solder resist layer including said metal wiring, and has projected caudad is included further.
[0029] two or more conductors which penetrated said resin object from the top face of said metal wiring, and were prolonged up in another desirable gestalt, and upper limit has exposed to the top face of this resin object -- a column is included further. according to this gestalt, a semiconductor device carries out a laminating to two or more layers -- having -- the

semiconductor devices of each class -- said conductor -- the component laminating mold semiconductor device mutually connected electrically through the above-mentioned connection bump on the upper limit of a column and the inferior surface of tongue of said metal wiring is obtained easily.
[0030] other desirable gestalten -- setting -- said conductor -- the side face of a column is exposed to the side face of said resin object. the conductor which the semiconductor devices which the semiconductor device is mutually connected on the side face according to this gestalt, and adjoin the side exposed to the side face of said resin object -- the component parallel connected type semiconductor device mutually connected electrically on the side faces of a column is obtained easily.
[0031] furthermore, another desirable gestalt -- setting -- said conductor -- the side face of a column is exposed to the side face of said resin object. the laminating of the semiconductor device is carried out to two or more layers by this gestalt, and it connects mutually on a side face -- having -- **** -- the semiconductor devices of each class -- said conductor -- the conductor which the semiconductor devices which are electrically connected mutually through the connection bump on the upper limit of a column and the inferior surface of tongue of said metal wiring, and adjoin the side exposed to the side face of said resin object -- the component laminating parallel connected type semiconductor device mutually connected electrically on the side faces of a column is obtained easily.
[0032] according to each above-mentioned ** better ****** -- each semiconductor device -- inspecting -- an excellent article -- choosing -- a laminating -- and/or, since side connection can be made and the semiconductor device of a component laminating mold, a component parallel connected type, and a component laminating parallel connected type can be manufactured, the product yield can be raised further.
[0033] In one gestalt, the capacitor which the closure is carried out to the interior of said resin object, and is carrying out direct continuation to this metal wiring can be included further. Desirably, said capacitor is an opposite monotonous mold and its plate surface of each plate is perpendicular to the thickness direction of said resin object.
[0034] one gestalt -- setting -- said resin -- the inorganic filler is distributing inside of the body. Thereby, the coefficient of thermal expansion and thermal conductivity of a resin object can be prepared to a request value.
[0035]
[Example] Hereafter, with reference to an accompanying drawing, an example explains this invention to a detail.
[Example 1] (1) sectional view and (2) plans show an example of the semiconductor device by the 1st invention to drawing 3 (1) and (2), respectively.
[0036] A semiconductor device 23 exposes tooth-back 23B up, and the illustrated semiconductor device 20 turns active side 23A to the top face of the insulating tape base material 21 which has the through tube 22 of the thickness direction caudad, and is joined to it. The closure resin layer 24 is formed in tape base material top-face field 21Y other than field 21X to which the semiconductor device 23 was joined, it gets down to it, and the perimeter of a side face of a semiconductor device 23 is closed. The metal wiring 25 formed in the inferior surface of tongue of the tape base material 21 took up the lower limit of the through tube 22 of the tape base material 21, and has demarcated the pars basilaris ossis occipitalis. The solder resist layer 26 which has the through tube 27 of the thickness direction has covered the inferior surface of tongue of the metal wiring 25 and the tape base material 21. From the inferior surface of tongue of the metal wiring 25, the eminent external connection terminal 28 was filled up with the through tube 27 of a solder resist layer 26, and penetrated, and it has projected caudad. The connection terminal 29 caudad prolonged from active side 23A of a semiconductor device 23 is inserted into the through tube of the tape base material 21. The connection terminal 29 and the metal wiring 25 are electrically connected by the filler 30 of the low-melt point point metal with which the gap of the connection terminal 29 and the wall of the through tube 22 of the tape base material 21 was filled up.
[0037] As a filler 30, it may replace with a low-melt point point metal, and conductive paste may

be used. Generally as conductive paste, the silver paste or copper paste which distributed the particle of silver or copper is used into polyimide resin or an epoxy resin. It is filled up with these conductive paste in a through tube by screen-stencil etc. Although the tooth back of a semiconductor device 23 and the top face of the closure resin layer 24 are on the same flat surface in the example of illustration, as long as the closure resin layer 24 is closing the perimeter of a side face of a semiconductor device 23, it is not necessary to be necessarily the same flat surface, and the height of the closure resin layer 24 may be lower than the tooth back of a semiconductor device 23 by the part distant from the side face of a semiconductor device 23.

[0038] An example of the manufacture approach of the semiconductor device of the 1st invention shown in drawing 3 is explained below with reference to drawing 4 - drawing 9 . The initial structure first prepared for drawing 4 is shown. The tape base material 21 had the area which may include two or more semiconductor package units, and equips the inferior surface of tongue with the metal wiring layer 25 and the solder resist layer 26. As a tape base material 21, although various kinds of organic materials or polymeric materials can be used, a resin film or resin sheets, such as an epoxy film generally strengthened with fiber, such as a polyimide film, glass, and aramid, or BT (bismaleimide triazine) film, and a PPE (polyphenylene ether) film, are suitable. As long as reinforcement and rigidity required as a base material are secured, the thinner one of the thickness of the tape base material 21 is desirable for thin-shape-izing of a semiconductor device, and generally range [of 25 micrometers - 100 micrometers], especially 75-micrometer order is used.

[0039] After forming a through tube 22 in the tape base material 21 by punching etc., the copper foil for forming the metal wiring layer 25 in one side is stuck. Or the hole which penetrates the tape base material 21 and makes copper foil a pars basilaris ossis occipitalis may be formed using the tape with copper foil on which the tape base material 21 and copper foil were unified by performing laser beam machining to tape base material 21 part. The tape with copper foil forms an insulating layer in copper foil by spreading of resin, such as polyimide.

[0040] Next, the through tube 22 (a pars basilaris ossis occipitalis demarcates by the metal wiring layer 25) of the tape base material 21 is imperfectly filled up with the filler 30 of a low-melt point point metal. That is, when the connection terminal 29 of a semiconductor device 21 is inserted at a back process, a filler 30 makes the gap of the connection terminal 29 and the wall of a through tube 22 a fill of a through tube 22 which is mostly filled to upper limit. As a low-melt point point metal of a filler 30, a silver-tin alloy (Ag-Sn), a lead-tin alloy (Pb-Sn), a silver-tin-copper alloy (Ag-Sn-Cu), the alloy that contains a bismuth (Bi) and antimony (Sb) in these can be used. Although it is desirable to carry out with the electrolysis plating which used copper foil as an electric supply layer as for restoration, screen-stencil of soldering paste can also perform it.

[0041] Subsequently, patterning of the above-mentioned copper foil is carried out by etching, and the metal wiring layer 25 is formed. The solder resist layer 26 which has a through tube 27 after formation of the metal wiring layer 25 is formed. Generally spreading of a photosensitive resist, exposure, and development perform formation of the solder resist layer 26 which has a through tube 27. It is few, and the number (number of a through tube 27) of an external connection terminal can carry out by screen-stencil of resin, when the pitch between external connection terminals is sufficiently large. The through tube 27 of a solder resist layer 26 is formed peripheral one or in the shape of an area array according to the application of the semiconductor device 20 to manufacture.

[0042] Next, as shown in drawing 5 , liquefied or the insulating coating 31 which consists of the resin of a semi-hardening condition is applied to the top face of the tape base material 21. The insulating coating 31 of a semi-hardening condition has the operation which pastes up a semiconductor device. Subsequently, as shown in drawing 6 , on the coating 31 before hardening, a semiconductor device 23 is arranged and it joins. namely, the through tube 22 to which the tape base material 21 corresponds the connection terminal 29 of the semiconductor device 23 of the need [of constituting two or more semiconductor package units] number -- respectively -- inserting -- the gap of the connection terminal 29 and the wall of a through tube 22 -- a through

tube 22 -- while making it mostly filled up with the low-melt point point metal 30 to upper limit, a semiconductor device 23 is joined and carried in the top face of the tape base material 21. This heats a semiconductor device 23 to the temperature near the melting point of the low-melt point point metal 30, and performs it by pushing in the connection terminal 29 into the low-melt point point metal 30 in a through tube 22.

[0043] As for the connection terminal 29 of a semiconductor device 23, forming as a bump of gold or copper is desirable. In the case of the semiconductor device 23 by which the connection terminal 29 is arranged to the periphery field, the connection terminal 29 is formed as a stud bump who generally used the wirebonding method. It is desirable to form the connection terminal 29 by the galvanizing method from a viewpoint which avoids the mechanical shock by stud bump formation in the case of the semiconductor device 23 by which the connection terminal 29 is arranged to the active field of a center section. The galvanizing method is advantageous especially when forming a bump in the shape of an area array with the rewiring section on a semiconductor device. As for a stud bump, forming withgold is desirable, and, as for a plating bump, it is desirable to form as a copper post equipped with the protection plating layer.

[0044] The size of the connection terminal 29, i.e., a bump, can be set as arbitration according to the design thickness of a semiconductor device 20. In an example, the diameter of a pars basilaris ossis occipitalis of a bump 29 is 30-60 micrometers in 70 micrometers and height. In that case, if the positioning accuracy in a bump's 29 formation is taken into consideration, the range of about 90-150-micrometer diameter is suitable for the through tube 22 of the tape base material 21 with which a bump 29 is inserted.

[0045] Next, as shown in drawing 7 , the closure resin layer 24 which covers the top face of tape base materials 21 other than the field in which the semiconductor device 23 was carried, and closes the perimeter of a side face of a semiconductor device 23 at least is formed. In addition, in drawing 7 - drawing 9 , the very thin insulating coating 31 was illustrated as the closure resin layer 24 and one, and separate illustration omitted it. The closure resin layer 24 also covered the semiconductor device 23 in drawing 7 , and showed the mode by which the whole is mostly formed in the same thickness to it. However, as another mode, as shown in drawing 8 , in this process step, the closure resin layer 24 may be thinner in the field which a semiconductor device 23 did not necessarily need to be covered, and the contact section with the side face of a semiconductor device 23 made thickness of the closure resin layer 24 equivalent to the height of a semiconductor device 23, and is distant from a semiconductor device 23 than this. Namely, what is necessary is just to set up the thickness of the closure resin layer 24 formed by this process step so that it may remain after the grinding performed at degree process, and polish by the thickness which can close completely the perimeter of a side face of a semiconductor device 23.

[0046] next, it is shown in drawing 9 -- as -- a part for the tooth-back 23B flank of the upper part of the closure resin layer 24, and a semiconductor device 23 -- grinding -- and it grinds and considers as predetermined thickness. Thereby, the semiconductor device 23 which was about 500 micrometers in the state of drawing 7 or drawing 8 can be made thin to about 50-100 micrometers. Consequently, a semiconductor device 20 is thinly made in about 120-300 micrometers. This is 1/4 or less thickness as compared with about 1200 micrometers in thickness of TSOP (Thin-Small-Outline Package) currently conventionally used abundantly most.

[0047] After grinding and polish, the external connection terminal 28 which projected from the inferior surface of tongue of a solder resist layer 26 is formed in the through tube 27 of a solder resist layer 26. This is performed by carrying out a reflow loading of a solder ball or after screen-stencil of soldering paste. Each semiconductor device 20 (drawing 3) is obtained by finally carving into drawing 9 per [u] semiconductor package in each location shown with the broken line.

[0048] [Example 2] (1) sectional view and (2) plans show other examples of the semiconductor device by the 1st invention to drawing 10 (1) and (2), respectively. The same reference number as the inside of drawing 3 was given to the structure of the example 1 shown in drawing 3 , and a corresponding part. In addition to the structure shown in drawing 3 , the illustrated

semiconductor device 40 contains further the conductor (conductor column) 32 of a low-melt point point metal. The conductor 32 penetrated the tape base material 21 of the field in which the closure resin layer 24 and the closure resin layer 24 which close the perimeter of a side face of a semiconductor device 23 are formed, upper limit was exposed to the top face of the closure resin layer 24, and the lower limit has connected it to the metal wiring layer 25 electrically.
[0049] As shown in drawing 11 , two or more layer laminating of the semiconductor device 40 of drawing 10 is carried out, and it can form the thin laminating mold semiconductor device 44 advantageously. That is, one semiconductor device 44 which consists of the circuit of one which contains the semiconductor device 23 of plurality (this example three pieces) as the whole laminated structure is constituted by connecting the upper limit of the conductor 32 of the low-melt point point metal of the lower layer semiconductor device 40, and the lower limit of the external connection terminal 28 of the upper semiconductor device 40. The laminating of a semiconductor device 40 can be performed as follows.
[0050] That is, a laminating mold semiconductor device is obtained by carrying out a reflow collectively, where it carried out the laminating, positioning two or more semiconductor devices with the fixture (appearance guide) which has the appearance of a semiconductor device and the load of the suitable load for the direction of a laminating is carried out. Or where it carried out the laminating of two or more semiconductor devices, positioning through a pin to the guide hole prepared in each semiconductor device and the load of the suitable load for the direction of a laminating is carried out, a reflow may be carried out collectively.
[0051] An example of the manufacture approach of the semiconductor device of the 1st invention shown in drawing 10 is explained below with reference to drawing 12 -16. The same reference number as the inside of drawing 4 - drawing 9 was given to the part corresponding to the structure of the example 1 shown in drawing 4 - drawing 9 . The initial structure shown in drawing 12 is the same as the initial structure of the example 1 shown in drawing 4 , except that the through tube 33 other than a through tube 22 is formed in the tape base material 21. The through tube 22 is formed in the location corresponding to the connection terminal 29 of a semiconductor device 23 like the example 1, and the through tube 33 is formed in the formation field of the closure resin layer 24 which closes the perimeter of a side face of a semiconductor device 23. Usually, a through tube 33 is magnitude it is several times whose diameter of this to a through tube 22. For example, a through tube 33 is about 500 micrometers in diameter to a through tube 22 being the diameter of about 25-100 micrometers. In the through tube 33 which had the base demarcated by the metal wiring layer 25, a small amount of flux 34 is arranged. About other parts of the initial structure shown in drawing 12 , it forms by the same processing as an example 1.
[0052] Next, as shown in drawing 13 , the conductor 32 of the low-melt point point metal which projected from the top face of the closure resin layer 24 is formed in a through tube 33. This is performed by carrying and carrying out a reflow of the ball (for example, solder ball) of a low-melt point point metal on the flux 34 in a through tube 33. Then, the insulating coating 31 is formed like an example 1.
[0053] Next, as shown in drawing 14 , like an example 1, on the coating 31 before hardening, a semiconductor device 23 is arranged and it joins. In connection with this, the connection terminal 29 which upheaved from AKUTIGU side 23A of a semiconductor device 23 is inserted into the through tube 22 of the tape base material 21, and is pushed in into the low-melt point point metal 30. Next, as shown in drawing 15 , the closure resin layer 24 which covers the top face of tape base materials 21 other than the field in which the semiconductor device 23 was carried, and closes the perimeter of a side face of a semiconductor device 23 at least is formed. In drawing 15 - drawing 16 , the insulating coating 31 omitted illustration.
[0054] The closure resin layer 24 also covered the semiconductor device 23 in drawing 15 , and showed the mode by which the whole is mostly formed in the same thickness to it. However, as the example 1 was shown in drawing 8 , in this process step, the closure resin layer 24 may be thinner than this in the field which a semiconductor device 23 did not necessarily need to be covered, and the contact section with the side face of a semiconductor device 23 made thickness of the closure resin layer 24 equivalent to the height of a semiconductor device 23,

and is distant from a semiconductor device 23. Namely, what is necessary is just to set up the thickness of the closure resin layer 24 formed by this process step so that it may remain after the grinding performed at degree process, and polish by the thickness which can close completely the perimeter of a side face of a semiconductor device 23.
[0055] next, it is shown in drawing 16 -- as -- a part for the tooth-back 23B flank of the upper part of the closure resin layer 24, the crowning of a conductor 32, and a semiconductor device 23 -- grinding -- and it grinds and considers as predetermined thickness. After grinding and polish, the external connection terminal 28 is formed like an example 1 in the through tube 27 of a solder resist layer 26. Each semiconductor device 40 (drawing 10) is obtained by finally carving into drawing 16 per [u] semiconductor package in each location shown with the broken line.
[0056] [Example 3] (1) sectional view and (2) plans show another example of the semiconductor device by the 1st invention to drawing 17 (1) and (2), respectively. The same reference number as the inside of drawing 3 was given to the structure of the example 1 shown in drawing 3 , and a corresponding part. The insulating frame 36 which replaces the illustrated semiconductor device 60 with the closure resin layer 24 in the structure shown in drawing 3 , is joined to tape base material 21 top faces other than the field in which the semiconductor device 23 was carried, and encloses the side face of a semiconductor device 23 through Gap G, The closure resin layer 24 which is filled up with the inside of Gap G and closes the perimeter of a side face of a semiconductor device 23 is included. The tape base material 21 of a field to which the frame 36 and the frame 36 are joined is penetrated, upper limit is exposed to the top face of a frame 36, and a lower limit is the structure which contains further the conductor (conductor column) 32 of the shape of a column of the low-melt point point metal electrically connected to the metal wiring layer 25.
[0057] As shown in drawing 18 , two or more layer laminating of the semiconductor device 60 of drawing 17 is carried out, and it can form the thin laminating mold semiconductor device 66 advantageously. That is, one semiconductor device 66 which consists of the circuit of one which contains the semiconductor device 23 of plurality (this example three pieces) as the whole laminated structure is constituted by connecting the upper limit of the conductor 32 of the shape of a column of the low-melt point point metal of the lower layer semiconductor device 60, and the lower limit of the external connection terminal 28 of the upper semiconductor device 60. The laminating of a semiconductor device 60 can be performed like an example 2.
[0058] An example of the manufacture approach of the semiconductor device 60 of the 1st invention shown in drawing 17 is explained below with reference to drawing 19 -22. The same reference number as the inside of drawing 4 - drawing 9 was given to the part corresponding to the structure of the example 1 shown in drawing 4 - drawing 9 . In addition to the structure shown in drawing 4 , the insulating base material 36 which has opening 37 is joined by the field which carries a semiconductor device 23 in the top face of the tape base material 21, the initial structure shown in drawing 19 penetrates the tape base material 21 and the insulating base material 36, and the column-like conductor 32 is formed. Opening 37 has the configuration and dimension which can hold a semiconductor device 23 through Gap G, as shown in drawing 17 (2). The through tube 22 of the tape base material 21 is formed in the location corresponding to the connection terminal 29 of a semiconductor device like the example 1.
[0059] The insulating base material 36 has the shape of a tape of the same appearance as the tape base material 21, and after it forms opening 37 by punching etc., it is joined to the top face of the tape base material 21. then, pillar-shaped -- opening of the through tube which penetrates the insulating base material 36 and the tape base material 21 by laser processing in the location which forms a conductor 32 is carried out. subsequently, pillar-shaped by the **** plating using copper foil before carrying out patterning to the metal wiring layer 25 as an electric supply layer -- a conductor 32 is formed. About other parts of the initial structure of drawing 19 , it forms by the same processing as an example 1. usually, pillar-shaped -- a conductor 32 is magnitude it is several times whose diameter of this to a through tube 22. for example, pillar-shaped to a through tube 22 being the diameter of about 25-100 micrometers -- a conductor 32 is about 500 micrometers in diameter. Next, as shown in drawing 20 , after forming the insulating

coating 31 in the top face of the tape base material 21 exposed in opening 37, like an example 1, on the coating 31 before hardening, a semiconductor device 23 is arranged and it joins. In connection with this, the connection terminal 29 which upheaved from AKUTIGU side 23A of a semiconductor device 23 is inserted into the through tube 22 of the tape base material 21, and is pushed in into the low-melt point point metal 30.

[0060] Next, as shown in drawing 21 , the gap G of a semiconductor device 23 and the opening 37 of the insulating base material 36 is closed in the closure resin layer 24. Thereby, the closure of the side face perimeter of a semiconductor device 23 is carried out. In drawing 21 - drawing 22 , the insulating coating 31 omitted illustration. next, it is shown in drawing 22 -- as -- a part for the tooth-back 23B flank of the upper part of the insulating base material 36, the upper part of the closure resin layer 24, the crowning of a conductor 32, and a semiconductor device 23 -- grinding -- and it grinds and considers as predetermined thickness.

[0061] After grinding and polish, the external connection terminal 28 is formed like an example 1 in the through tube 27 of a solder resist layer 26. Each semiconductor device 60 (drawing 17) is obtained by finally carving into drawing 22 per [u] semiconductor package in each location shown with the broken line.

[Example 4] The structure before carving manufactured using the thing of the shape of a disk from the diameter of 2 inches to 12 inches as initial structure which contains the tape base material 21 in drawing 23 is shown. Since a facility of the existing grinding machine, a cutting machine, etc. which process the semi-conductor wafer of the same size by using such a configuration and the initial structure of a dimension can be used, the costs for the part and a new facility can be reduced. Although the case where the semiconductor device of the structure of an example 3 was manufactured was shown in drawing 23 , of course, it is applicable similarly [in the case of an example 1 and an example 2].

[0062] [Example 5] (1) sectional view, (2) sectional views, and (3) plans show an example of the semiconductor device by the 2nd invention to drawing 24 (1), (2), and (3), respectively. The reference number which added 100 to the reference number in these examples was given to the structure of examples 1-4, and a corresponding part (also setting in the subsequent examples the same). The metal wiring 125 is formed in the top face of the insulating tape base material 121, and a semiconductor device 123 exposes tooth-back 123B up, and the illustrated semiconductor device 101 turns active side 123A caudad, and is carried. The lower limit of the connection terminal 129 which projected from active side 123A of a semiconductor device 123 to the lower part has connected with the top face of the metal wiring 125. The closure resin layer 124 formed in the top face of the tape base material 121 closed the perimeter of a side face of a semiconductor device 123, and is filled up with the gap of active side 123A of a semiconductor device 123, and the top face of the tape base material 121.

[0063] a conductor -- the column 132 was prolonged in the upper part from the top face of the metal wiring 125, and penetrated the closure resin layer 124 around [side face] a semiconductor device 123, and upper limit is exposed up. a conductor -- a column 132 may be a ball-like (the shape of an entasis [Correctly]) mostly, as shown in drawing 24 (1), and as shown in drawing 24 R> 4 (2), it may be straight-rod shape. a conductor -- columns 132 are a metaled column or metaled balls, such as copper or nickel, and are the balls of low-melt point point metals, such as solder, desirably. As this solder, a silver-tin alloy (Ag-Sn), a lead-tin alloy (Pb-Sn), a silver-tin-copper alloy (Ag-Sn-Cu), and the solder that contains a bismuth (Bi) and antimony (Sb) in these can be used.

[0064] With reference to drawing 25 , the manufacture approach of the semiconductor device 101 shown in drawing 24 is explained. This example can be applied when manufacturing collectively about many semiconductor package units like examples 1-4, but in order to give explanation brief below, it is explained in the form manufactured about a single semiconductor package unit. First, as shown in drawing 25 (1), the semiconductor device 123 which equipped active side 123A with the connection terminal 129, and the tape base material 121 which equipped the top face with the metal wiring 125 are prepared. The formation approach of the connection terminal 129, the ingredient configuration of the tape base material 121, and the formation approach of the metal wiring 125 are the same as that of an example 1.

[0065] Next, as shown in drawing 25 (2), a semiconductor device 123 is carried in the top face of the tape base material 121 by joining the connection terminal 129 of active side 123A of a semiconductor device 123 to the top face of the metal wiring 125 of the tape base material 121. This junction (loading) can be performed as follows. The connection terminal 129 which carries out the heating pressure welding of the connection terminal 129 to the metal (solder) layer formed in the predetermined location of the metal wiring 125 with plating etc. beforehand, or consists of a golden bump on gilding on the metal wiring 125 is carried, and it joins through direct junction, or an anisotropic conductive film or a paste by ultrasonic impression.
[0066] next, the conductor which the lower limit joined to the top face of the metal wiring 125 as shown in drawing 25 (3) -- a column 132 is formed. the example of illustration -- a conductor -- the column 132 was shown in drawing 24 (2) -- it is a ball-like (the shape of an entasis [Correctly]) mostly, and is a solder ball. the conductor using a solder ball -- formation of a column 132 can be performed by carrying out a reflow, after carrying a solder ball in the predetermined part of metal wiring 125 top face or screen-stenciling soldering paste. a conductor -- a column 132 may be the straight-rod shape shown in drawing 24 (2). a straight-rod shaped conductor -- formation of a column 132 can be performed as follows. Preferably, the rod-like structure of copper ** was joined to the predetermined part of metal wiring 125 top face by heating pressurization, solder etc. was beforehand galvanized in the predetermined part of metal wiring 125 top face, and also [the metal which performed solder plating, tin (Sn) plating, indium (In) plating, etc. to the front face, and] the above-mentioned rod-like structure is carried, and a reflow is carried out.
[0067] Next, as shown in drawing 25 (4), the closure resin layer 124 is formed. the closure resin layer 124 -- the metal wiring 125 and a conductor -- the perimeters of a side face of a semiconductor device 123 including a column 132 are closed, and it is filled up with the gap of active side 123A of a semiconductor device 123, and the top face of the tape base material 121. Molding or potting can perform formation of the closure resin layer 124.
[0068] next, it is shown in drawing 25 (5) -- as -- a part for the tooth-back flank of the upper part of the closure resin layer 124, and a semiconductor device 123 -- grinding -- and -- grinding -- given thickness -- ** -- carrying out -- a conductor -- the upper limit of a column 132 is exposed up. the whole which the need does not have and not necessarily includes a semiconductor device 123 by the grinding and polish of drawing 25 R> 5 (5) although the top face of the closure resin layer 124 was made into the same flat surface as the top face (tooth back) of a semiconductor device 123 at the process of drawing 25 (4) -- given thickness -- ** -- the time of carrying out -- a conductor -- what is necessary is just to set up the thickness of the closure resin layer 124 so that the upper limit of a column 132 may be up exposed
[0069] Although only the single semiconductor package unit was shown in drawing 25 , many semiconductor package units can be collectively manufactured by performing the process of drawing 25 (1) - (5) using the tape base material 121 of the area which may include two or more semiconductor device package units in fact. In that case, finally the tape base material 121 can be carved per semiconductor package, and each semiconductor device 101 (drawing 24 R> 4) can be obtained.
[0070] [Example 6] (1) sectional view and (2) plans show other examples of the semiconductor device by the 2nd invention to drawing 26 (1) and (2), respectively. the semiconductor device 102 of this example -- setting -- the conductor of an example 5 -- instead of the column 132, the external connection terminal 128 was caudad prolonged from the inferior surface of tongue of the metal wiring 125, penetrated the tape base material 121, and it has projected caudad. It is the same structure as an example 5 except it. the ingredient of the external connection terminal 128 -- a conductor -- it can choose from the same ingredient as using for a column 132.
[0071] With reference to drawing 27 , the manufacture approach of the semiconductor device 102 shown in drawing 26 is explained. This example can be applied when manufacturing collectively about many semiconductor package units like examples 1-4, but in order to give explanation brief below, it is explained in the form manufactured about a single semiconductor package unit. First, as shown in drawing 27 (1), the semiconductor device 123 which equipped active side 123A with the connection terminal 129, and the tape base material 121 are prepared.

The tape base material 121 equipped the top face with the metal wiring 125, had through tube 121H of the thickness direction in the location corresponding to the external connection terminal 128, closed the upper limit whose inferior surface of tongue of the metal wiring 125 is through tube 121H, and has demarcated them. The formation approach of the connection terminal 129, the ingredient configuration of the tape base material 121, and the formation approach of the metal wiring 125 are the same as that of an example 1. The formation approach of through tube 121H is the same as that of the through tube 22 of an example 1.

[0072] Next, as shown in drawing 27 (2), a semiconductor device is carried in the top face of the tape base material 121 like the process of drawing 25 (2) of an example 5.

[0073] Next, as shown in drawing 27 (3), the closure resin layer 124 is formed like the process of drawing 25 (4) of an example 5.

[0074] next, it is shown in drawing 27 (4) -- as -- a part for the tooth-back flank of the upper part of the closure resin layer 124, and a semiconductor device 123 -- grinding -- and -- grinding -- given thickness -- ** -- it carries out. the whole which the need does not have and not necessarily includes a semiconductor device 123 by next grinding and polish although considered as the condition that the top face of the closure resin layer 124 was higher than the top face (tooth back) of a semiconductor device 123, and the semiconductor device 123 whole was embedded to the interior of the closure resin layer 124, at the process of drawing 27 (3) -- given thickness -- ** -- what is necessary is just to set up the thickness of the closure resin layer 124 so that it can carry out

[0075] Next, as shown in drawing 27 (5), the external connection terminal 128 is formed. The external connection terminal 128 was caudad prolonged from the inferior surface of tongue of the metal wiring 125 which demarcates the upper limit of through tube 121H, was filled up with through tube 121H, and has projected them caudad. This order is sufficient as the sequence of the grinding and the polish process of drawing 27 (4), and the external connection terminal formation process of drawing 27 (5), and a reverse order is sufficient as it.

[0076] Although only the single semiconductor package unit was shown in drawing 27 , many semiconductor package units can be collectively manufactured by performing the process of drawing 27 (1) - (5) using the tape base material 121 of the area which may include two or more semiconductor device package units in fact. In that case, finally the tape base material 121 can be carved per semiconductor package, and each semiconductor device 102 (drawing 26 R> 6) can be obtained.

[0077] [Example 7] (1) sectional view and (2) plans show another example of the semiconductor device by the 2nd invention to drawing 28 (1) and (2), respectively. the semiconductor device 103 of this example -- setting -- the conductor of an example 5 -- both the column 132 and the external connection terminal 128 of an example 6 are formed. The method of manufacturing the semiconductor device 103 of this example is an approach which combined the production process of an example 5, and the production process of an example 6. With reference to drawing 25 and drawing 27 , the manufacture approach of the semiconductor device 103 shown in drawing 28 is explained. Two or more layer laminating of the semiconductor device 103 shown in drawing 28 can be carried out, and it can be used.

[0078] First, the semiconductor device 123 and the tape base material 121 which are shown in drawing 27 (1) are prepared like an example 6, and as shown in drawing 2727 (2), a semiconductor device is carried in the top face of the tape base material 121.

[0079] next, the conductor which the lower limit joined to the top face of the metal wiring 125 as shown in drawing 25 (3) -- a column 132 is formed, and as shown in drawing 25 (4), the closure resin layer 124 is formed. Then, the semiconductor device 103 of drawing 28 is obtained by performing the grinding and the polish process of drawing 27 (4), and the external connection terminal formation process of drawing 27 (5) by this order or reverse order.

[0080] Although the single semiconductor package unit was explained here, many semiconductor package units can be collectively manufactured by performing the above-mentioned process using the tape base material 121 of the area which may include two or more semiconductor device package units in fact. In that case, finally the tape base material 121 can be carved per semiconductor package, and each semiconductor device 103 (drawing 28) can be obtained.

[0081] The semiconductor device by the 1st invention and the 2nd invention which were explained above is the structure containing a tape base material. The example of the semiconductor device by the 3rd invention of the structure which does not contain a tape base material in below is explained.
[Example 8] A sectional view shows an example of the semiconductor device by the 3rd invention to drawing 29 (1) and (2). The semiconductor device 123 exposed tooth-back 123B to the top face of the resin object 124 by carrying out the closure, and, as for the semiconductor device 104 shown in drawing 29 (1), the semiconductor device 123 has turned active side 123A to the interior of the resin object 124 of predetermined thickness caudad. The metal wiring 125 is formed in the inferior surface of tongue of the resin object 124, and the connection terminal 129 caudad prolonged from active side 123A of a semiconductor device 123 has connected with the top face of the metal wiring 125. Tooth-back 123B of the top face of the resin object 124 and a semiconductor device 123 has constituted the same flat surface. The connection terminal 129 can be formed as a golden stud bump, a plating bump, etc.
[0082] In the structure of the semiconductor device 104 of drawing 29 (1), the solder resist layer 126 has covered the inferior surfaces of tongue of the resin object 124 including the metal wiring 125, the connection bump 128 formed in the inferior surface of tongue of the metal wiring 125 penetrated the solder resist layer 126, and semiconductor device 104' shown in drawing 29 (2) has projected caudad.
[0083] With reference to drawing 30 , the manufacture approach of the semiconductor device 104 shown in drawing 29 and 104' is explained. This example can be applied when manufacturing collectively about many semiconductor package units like examples 1-4, but in order to give explanation brief below, it is explained in the form manufactured about a single semiconductor package unit. First, as shown in drawing 30 (1), a semiconductor device 123 is carried on metal substrate 125M by joining to top faces of metal substrate 125M, such as aluminum foil, Cu foil, copper foil that formed wiring by gilding, and a Cu flare aluminum foil, by approaches, such as alloy junction which minded ultrasonic jointing and low-melt point point metals, such as an indium, for the tip of the connection terminal 129 formed in active side 123A of a semiconductor device 123.
[0084] Next, as shown in drawing 30 (2), the resin object 124 is formed by covering the whole top face of metal substrate 125M by resin. The resin object 124 is closing the semiconductor device 123 inside, and the inferior surface of tongue has joined it to metal substrate 125M. As a resin object 124, an epoxy resin, polyimide resin, cyano ester resin, and polycyclic aromatic series system resin can be used, and especially an epoxy resin is desirable. In order to adjust the coefficient of thermal expansion and thermal conductivity of the resin object 124, ceramic particles, such as a silica, an alumina, and alumimium nitride, can be distributed as an inorganic filler. Variance is set up according to a desired coefficient of thermal expansion and the value of thermal conductivity. Particle size is 2-10 micrometers. Particle shape is so desirable that it is spherically near.
[0085] Next, as shown in drawing 30 (3), the metal wiring 125 is formed in the inferior surface of tongue of the resin object 124 by carrying out patterning of metal substrate 125M. The top face has connected the metal wiring 125 to the connection terminal 129. a part for next, the tooth-back flank of the upper part of the resin object 124, and a semiconductor device 123 -- grinding -- and -- grinding -- given thickness -- ** -- it carries out. According to the above process, the semiconductor device 104 shown in drawing 29 (1) is completed.
[0086] Furthermore, it is the process of drawing 30 (3), next as shown in drawing 30 (4), the wrap solder resist layer 126 is formed for the whole inferior surface of tongue of the resin object 124 including the metal wiring 125, and a through tube 127 is formed in a solder resist layer 126. A lower limit carries out opening of the through tube 127, upper limit is closed by the inferior surface of tongue of the metal wiring 125, and it is demarcated.
[0087] next, it was shown in drawing 30 (5) -- as -- a part for the tooth-back flank of the upper part of the resin object 124, and a semiconductor device 123 -- grinding -- and -- grinding -- given thickness -- ** -- it carries out.
[0088] Next, as shown in drawing 30 (6), the external connection terminal 128 which was filled up

with the through tube 127 and projected caudad is formed. the conductor which this showed to drawing 25 (3) -- it carries out like a column 132 loading of a solder ball and by carrying out an after [soldering paste printing] reflow. In addition, the grinding and the polish process of drawing 30 (5), and the external connection terminal formation process of drawing 30 (6) may be performed to a reverse order. Thereby, semiconductor device 104' shown in drawing 29 (2) is completed.

[0089] Although the single semiconductor package unit was explained here, many semiconductor package units can be collectively manufactured by performing the above-mentioned process using metal substrate 125M of the area which may include two or more semiconductor device package units in fact. In that case, finally metal substrate 125M can be carved per semiconductor package, and each semiconductor device 104 or 104' (drawing 29) can be obtained.

[0090] Next, with reference to drawing 31 , other manufacture approaches of the semiconductor device 104 shown in drawing 29 and 104' are explained. First, as shown in drawing 31 (1), compound metal plate 125A which formed the circuit pattern 125 of a dissimilar metal in the top face of metal substrate 125M is produced. This is performed by forming the Cu circuit pattern 125 on aluminum substrate 125M by forming the Au circuit pattern 125 with Au plating on Cu substrate 125M which consist of Cu foil, or etching and carrying out patterning of the Cu of a Cu flare aluminum foil.

[0091] Next, as shown in drawing 31 (2), a semiconductor device 123 is carried on compound metal plate 125A by joining to the top face of a circuit pattern 125 by approaches, such as alloy junction which minded low-melt point point metals, such as ultrasonic jointing and an indium, for the tip of the connection terminal 129 formed in active side 123A of a semiconductor device 123.

[0092] Next, as shown in drawing 31 (3), the resin object 124 is formed by covering the whole top face of compound metal plate 125A including a circuit pattern 125 by resin. The resin object 124 is closing the semiconductor device 123 inside, and the inferior surface of tongue has joined it to a circuit pattern 125 and metal substrate 125M. The resin object 124 is the same quality of the material as the thing explaining drawing 30 (2).

[0093] Next, as shown in drawing 31 (4), etching removes metal substrate 125M. In the case of the combination of Au circuit pattern 125/Cu foil substrate 125M, although Cu is dissolved, specifically, Au removes Cu foil substrate 125M by etching using the etchant not dissolving. Or in the case of the combination of Cu circuit pattern 125/aluminum substrate 125M, although aluminum is dissolved, Cu removes aluminum substrate 125M by etching using the etchant not dissolving. The structure where the metal wiring 125 which consists of Au or Cu was joined to the inferior surface of tongue of the resin object 124 by this is acquired. a part for next, the tooth-back flank of the upper part of the resin object 124, and a semiconductor device 123 -- grinding -- and -- grinding -- given thickness -- ** -- it carries out. According to the above process, the semiconductor device 104 shown in drawing 29 (1) is completed. However, although the location of the plane of composition of the resin object 124 and a solder resist layer 126 serves as a top face of the metal wiring 125, and the same field with the structure of drawing 29 (1), they differ in the acquired structure which was acquired at the above-mentioned process at the point used as the inferior surface of tongue of the metal wiring 125, and the same field.

[0094] Furthermore, it is the process of drawing 31 (4), next the same procedure as the process which showed formation of a solder resist layer 126, grinding and polish, and formation of the external connection terminal 128 to drawing 30 (4), (5), and (6), respectively in the sequence shown in drawing 31 (5), (6), and (7) performs. Also in this case, the grinding and the polish process of drawing 31 (6), and the external connection terminal formation process of drawing 31 (7) may be performed to a reverse order. Semiconductor device 104' which this showed to drawing 29 (2) is completed. However, although the location of the plane of composition of the resin object 124 and a solder resist layer 126 serves as a top face of the metal wiring 125, and the same field with the structure of drawing 2929 (2), they differ in the acquired structure which was acquired at the above-mentioned process at the point used as the inferior surface of tongue of the metal wiring 125, and the same field.

[0095] [Example 9] A sectional view shows other examples of the semiconductor device by the 3rd invention to drawing 32 . drawing 32 -- (-- one --) -- (-- two --) -- (-- three --) -- respectively -- having been shown -- a semiconductor device -- 105 -- 105 -- ' -- 105 -- " -- each -- drawing 29 -- (-- one --) -- having been shown -- a semiconductor device -- 104 -- structure -- in addition, two or more conductors -- it has the column 132 further. a conductor -- from the top face of the metal wiring 125, the column 132 penetrated the resin object 124, and is prolonged up, and upper limit has exposed it to the top face of the resin object 124. here -- the semiconductor device 105 of drawing 32 (1) -- a conductor -- the upper limit of a column 132 -- from the resin object 124 -- exposing -- **** -- semiconductor device 105' of drawing 32 (2) -- a conductor -- the upper limit and side face of a column 132 are exposed from the resin object 124.

[0096] the conductor with which only upper limit has exposed semiconductor device 105" of drawing 32 (3) from the resin object 124 -- the conductor which column 132A, and upper limit and a side face have exposed from the resin object 124 -- it has column 132B and the wrap solder resist layer 126 is formed in the inferior surfaces of tongue of the resin object 124 including the metal wiring 125. however, the conductor with which the side face exposed the solder resist layer 126 -- the part of the metal wiring 125 linked to column 132B was not covered, but the inferior surface of tongue of the metal wiring 125 is exposed in this part. a conductor -- Columns 132, 132A, and 132B can be formed by low melting alloys, such as metals, such as copper (Cu), nickel (nickel), and covar (trade name), an alloy or a tin-silver (Sn-Ag) alloy, and a tin-lead (Sn-Pb) alloy.

[0097] the semiconductor device 105 shown in drawing 32 , 105', and the top face of metal substrate 125M used for the production process explained by drawing 30 R> 0 in the example 8 in order to manufacture 105" -- beforehand -- stud bump formation, junction of a metal column, etc. -- a conductor -- what is necessary is to form the column 132 and just to perform suitably the process of drawing 30 R> 0 as well as an example 8

[0098] [Example 10] The example of the component laminating mold semiconductor device which carried out two or more layer laminating of the semiconductor device 105 shown in drawing 32 (1) to drawing 33 is shown. After the illustrated semiconductor device 106 carries out the three-layer laminating of the semiconductor device 105 and forms a solder resist layer 126 and the connection bump 128 like drawing 29 (2) in addition to the structure of drawing 32 (1), the laminating of it is carried out and it is made into one. a lower layer conductor -- the upper limit of a column 132 and the inferior surface of tongue of the upper metal wiring 125 have connected mutually electrically through the connection bump 128.

[0099] [Example 11] The example of the component parallel connected type semiconductor device which connected to drawing 34 (1) mutually semiconductor device 105' shown in drawing 32 (2) on the side face is shown. the conductor which the illustrated semiconductor device 107 connected two semiconductor device 105' to juxtaposition, covered the inferior surfaces of tongue of the resin object 124 including the metal wiring 125 by the solder resist layer 126 except for the side edge section, and was exposed to the side face of the resin object 124 -- it connects mutually electrically through the low-melt point point metals 138, such as solder, on the side faces of a column 132. This connection can be made as follows. carrying out a reflow, after carrying a low-melt point point metal ball, or after supplying a low-melt point point metal by printing or dotting of a low-melt point point metal paste -- the low-melt point point metal 138 -- the metal wiring 125 and a conductor -- breadth and junction are performed to the exposure of a column 132. When spacing of a joint is large, it can also join by dotting of conductive paste.

[0100] The example of the component laminating parallel connected type semiconductor device which carried out the laminating of semiconductor device 105' shown in drawing 32 (2) to drawing 34 (2), and carried out parallel connection to it is shown. The two-layer laminating of the layer which connected two semiconductor device 105' to juxtaposition is carried out, and the illustrated semiconductor device 108 changes. The connection relation of each semiconductor device 105' is the relation which combined the component laminating mold semiconductor device 106 of drawing 33 , and the component parallel connected type semiconductor device 107 of drawing 34 (1).

[0101] [Example 12] The example of the semiconductor device of the 3rd invention which contains a capacitor in drawing 35 (1) is shown. In addition to the structure of semiconductor device 104' of drawing 29 (2), the illustrated semiconductor device 109 is equipped with the capacitor 143 by which the closure was carried out into the resin object 124. As for the capacitor 143, direct continuation of the electrode terminal 145 of two poles is carried out to the top face of the metal wiring 125. As shown in drawing 35 (2), a capacitor 143 is an opposite monotonous mold and its pattern side of each conductor pattern 147 is desirably parallel to the thickness direction of the resin object 124. It is the usual ceramic stacked capacitor and the capacitor 143 is filled up with a dielectric 149 like strontium titanate between conductor patterns 147. Since electrostatic capacity, i.e., effective area, is decided by thickness after grinding and polish, it is necessary to expect and design the last thickness.
[0102] As a capacitor 143, a commercial chip capacitor (chip capacitor) is used suitably. In addition, the structure containing a capacitor 143 is applicable not only to the semiconductor device shown in drawing 35 (1) but the semiconductor device shown in drawing 24 , drawing 29 (1), and drawing 32 R> 2.
[0103]
[Effect of the Invention] According to this invention, it equalizes at the same time it reduces installation height, and the complicated process for each chip installation is not needed, but the manufacture yield is improved, the height of a semiconductor device is equalized, without being influenced by thickness dispersion of a chip, and the semiconductor device and its manufacture approach as a thin semiconductor package in which package activation of an electric trial is possible are offered.

[Translation done.]

* NOTICES *

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1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] Drawing 1 is the perspective view showing the conventional semiconductor device after connecting the lead of TCP with a semiconductor chip, and shows the condition before cutting each TCP from a tape.
[Drawing 2] Drawing 2 is the sectional view in which expanding the core of the semiconductor device of drawing 1 , and showing the conventional semiconductor chip and the condition of connection of the lead of a package.
[Drawing 3] Drawing 3 (1) and (2) are the each (1) sectional view and (2) plans showing an example of the semiconductor device by the 1st invention.
[Drawing 4] Drawing 4 is the sectional view showing the initial structure prepared first, in order to manufacture the semiconductor device of the 1st invention shown in drawing 3 .
[Drawing 5] Drawing 5 is the sectional view showing the condition of having formed insulating coating in the initial structure shown in drawing 4 .
[Drawing 6] Drawing 6 is the sectional view showing the process which arranges a semiconductor device and is joined on coating before hardening.

[Drawing 7] Drawing 7 is the sectional view showing the condition of having formed the closure resin layer which covers the top face of tape base materials other than the field in which the semiconductor device was carried, and closes the perimeter of a side face of a semiconductor device at least.
[Drawing 8] Drawing 8 is the sectional view showing the condition of having formed the closure resin layer which covers the top face of tape base materials other than the field in which the semiconductor device was carried, and closes the perimeter of a side face of a semiconductor device at least by another mode with drawing 7 .
[Drawing 9] Drawing 9 is the sectional view showing grinding and the condition of having ground, having considered as predetermined thickness and having formed the external connection terminal for a part for the tooth-back flank of the upper part of a closure resin layer, and a semiconductor device.
[Drawing 10] Drawing 10 (1) and (2) are the each (1) sectional view and (2) plans showing other examples of the semiconductor device by the 1st invention.
[Drawing 11] Drawing 11 is the sectional view showing the thin laminating mold semiconductor device which carried out two or more layer laminating of the semiconductor device of drawing 10 , and formed it.
[Drawing 12] Drawing 12 is the sectional view showing the initial structure prepared first, in order to manufacture the semiconductor device of the 1st invention shown in drawing 10 .
[Drawing 13] Drawing 13 is the sectional view showing the condition of having formed the conductor and insulating coating of a low-melt point point metal in the initial structure shown in drawing 12 .
[Drawing 14] Drawing 14 is the sectional view showing the process which arranges a semiconductor device and is joined on coating before hardening.
[Drawing 15] Drawing 15 is the sectional view showing the condition of having formed the closure resin layer which covers the top face of tape base materials other than the field in which the semiconductor device was carried, and closes the perimeter of a side face of a semiconductor device at least.
[Drawing 16] Drawing 16 is the sectional view showing grinding and the condition of having ground, having considered as predetermined thickness and having formed the external connection terminal for a part for the tooth-back flank of the upper part of a closure resin layer, and a semiconductor device.
[Drawing 17] Drawing 17 (1) and (2) are (1) sectional view and (2) plans showing another example of the semiconductor device by the 1st invention, respectively.
[Drawing 18] Drawing 18 is the sectional view showing the thin laminating mold semiconductor device which carried out two or more layer laminating of the semiconductor device of drawing 17 , and formed it.
[Drawing 19] Drawing 19 is the sectional view showing the initial structure prepared first, in order to manufacture the semiconductor device of the 1st invention shown in drawing 17 .
[Drawing 20] Drawing 20 is the sectional view showing the process which forms insulating coating in the initial structure shown in drawing 19 , arranges a semiconductor device and is joined on coating before hardening.
[Drawing 21] Drawing 21 is the sectional view showing the condition of having closed the gap of a semiconductor device and opening of an insulating base material in the closure resin layer.
[Drawing 22] Drawing 22 is the sectional view showing grinding and the condition of having ground, having considered as predetermined thickness and having formed the external connection terminal, from the condition shown in drawing 21 for a part for the tooth-back flank of the upper part of an insulating base material, the upper part of a closure resin layer, and a semiconductor device.
[Drawing 23] Drawing 23 is the perspective view which was manufactured using a disk-like thing as initial structure containing a tape base material and in which carving into and showing a part of front structure in a cross section.
[Drawing 24] Drawing 24 (1), (2), and (3) are (1) sectional view, (2) sectional views, and (3) plans showing an example of the semiconductor device by the 2nd invention.

[Drawing 25] Drawing 25 is the sectional view showing the process for manufacturing the semiconductor device of drawing 24 (1).
[Drawing 26] Drawing 26 (1) and (2) are (1) sectional view and (2) plans showing other examples of the semiconductor device by the 2nd invention.
[Drawing 27] Drawing 27 is the sectional view showing the process for manufacturing the semiconductor device of drawing 26 .
[Drawing 28] Drawing 28 (1) and (2) are (1) sectional view and (2) plans showing another example of the semiconductor device by the 2nd invention.
[Drawing 29] Drawing 29 (1) and (2) are the sectional views showing an example of the semiconductor device by the 3rd invention.
[Drawing 30] Drawing 30 is the sectional view showing an example of the process for manufacturing the semiconductor device of drawing 29 .
[Drawing 31] Drawing 31 is the sectional view showing other examples of the process for manufacturing the semiconductor device of drawing 29 .
[Drawing 32] Drawing 32 (1), (2), and (3) are the sectional views showing other examples of the semiconductor device by the 3rd invention.
[Drawing 33] Drawing 33 is the sectional view showing the thin laminating mold semiconductor device which carried out two or more layer laminating of the semiconductor device of drawing 32 , and formed it.
[Drawing 34] Drawing 34 (1) and (2) are the sectional views showing the component parallel connected type semiconductor device which carried out (1) parallel connection of the semiconductor device of drawing 32 , (2) laminatings, and the component laminating parallel connected type semiconductor device which carried out parallel connection, respectively.
[Drawing 35] Drawing 35 is (1) sectional view and (2) partial expanded sectional view showing the example of the semiconductor device of the 3rd invention containing a capacitor.
[Description of Notations]
1 -- Resin film (base material)
2 -- Lead
3 -- Sprocket hole
4 -- Semiconductor chip (semiconductor device)
5 -- Opening (device hole)
6 -- Bumps (gold etc.)
7 -- Closure resin
10 -- The conventional TCP
20 -- Semiconductor device by the 1st invention
21 -- Insulating tape base material
22 -- Through tube of the thickness direction of the tape base material 21
23 -- Semiconductor device
23A -- Active side of a semiconductor device
23B -- Tooth back of a semiconductor device
24 -- Closure resin layer
25 -- Metal wiring
26 -- Solder resist layer
27 -- Through tube of the thickness direction of a solder resist layer
28 -- External connection terminal
29 -- Connection terminal of a semiconductor device
30 -- Filler of a low-melt point point metal
31 -- Insulating coating
32 -- Conductor of a low-melt point point metal (pillar-shaped conductor)
36 -- Insulating base material
37 -- Through tube of the thickness direction of the insulating base material 36
40 -- Semiconductor device by the 1st invention
44 -- Component laminating mold semiconductor device by the 1st invention
60 -- Semiconductor device by the 1st invention

66 -- Component laminating mold semiconductor device by the 1st invention
101 -- Semiconductor device by the 2nd invention
102 -- Semiconductor device by the 2nd invention
103 -- Semiconductor device by the 2nd invention
104 -- Semiconductor device by the 3rd invention
104' -- Semiconductor device by the 3rd invention
105 -- Semiconductor device by the 3rd invention
105' -- Semiconductor device by the 3rd invention
105" -- Semiconductor device by the 3rd invention
106 -- Component laminating mold semiconductor device by the 3rd invention
107 -- Component parallel connected type semiconductor device by the 3rd invention
108 -- Component laminating parallel connected type semiconductor device by the 3rd invention

109 -- Semiconductor device equipped with the capacitor by the 3rd invention
121 -- Insulating tape base material
121H -- Through tube of an insulating tape base material
123 -- Semiconductor device
123A -- Active side of a semiconductor device
123B -- Tooth back of a semiconductor device
124 -- Closure resin layer
125 -- Metal wiring (circuit pattern)
125A -- Compound metal plate
125M -- Metal substrate
126 -- Solder resist layer
127 -- Through tube of a solder resist layer
128 -- An external connection terminal or connection bump
129 -- Connection terminal of a semiconductor device
132 -- a conductor -- a column
132A-- a conductor -- a column
132B-- a conductor -- a column
143 -- Capacitor
145 -- Electrode terminal of a capacitor
147 -- Plate with which a capacitor counters
149 -- Dielectric which fills between the plates of a capacitor

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[Translation done.]

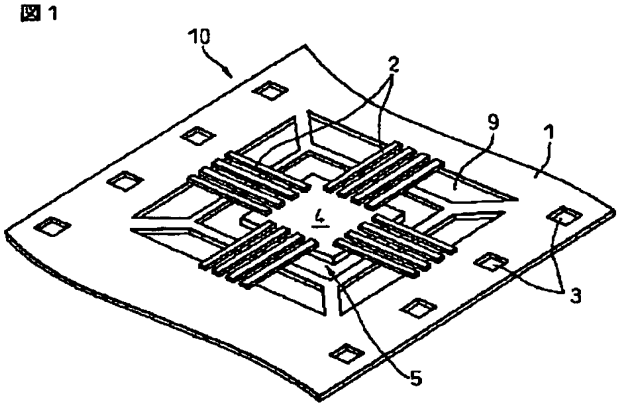
* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

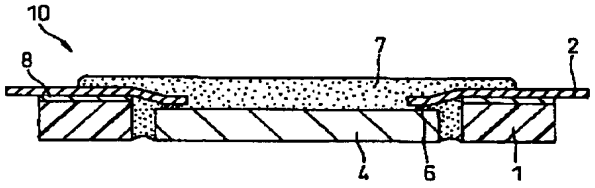
[Drawing 1]

図 1



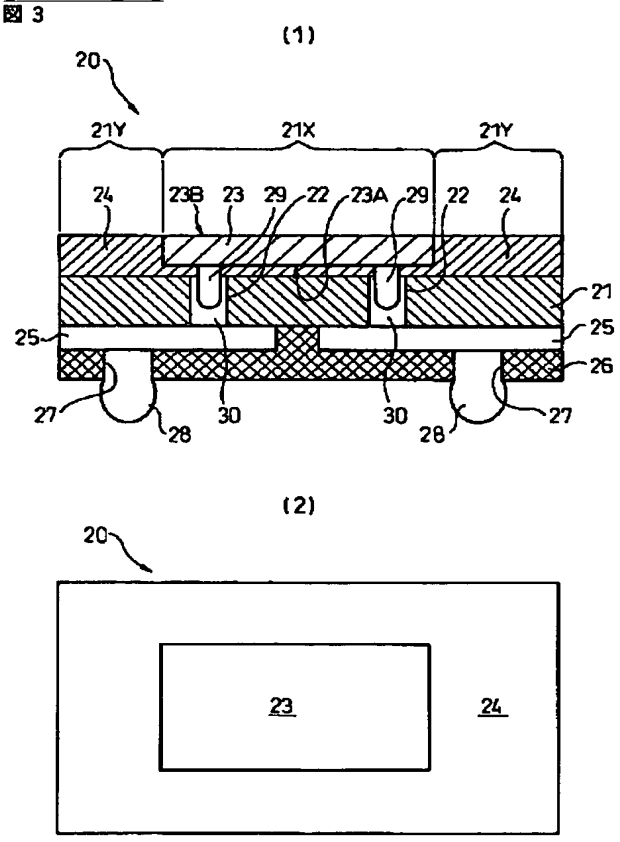
[Drawing 2]

図 2



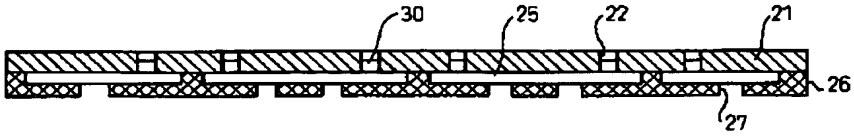
[Drawing 3]

図 3



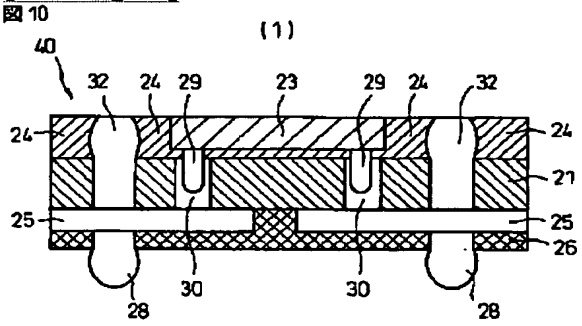
[Drawing 4]

図7



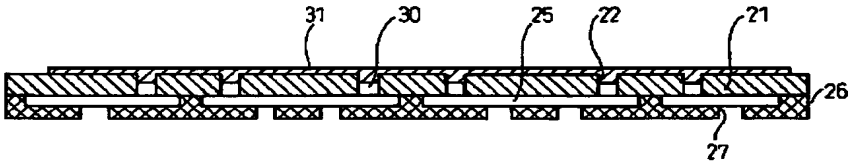
[Drawing 10]

図10



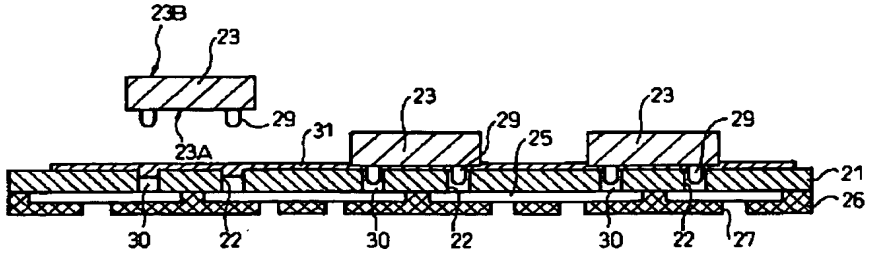
[Drawing 5]

図5



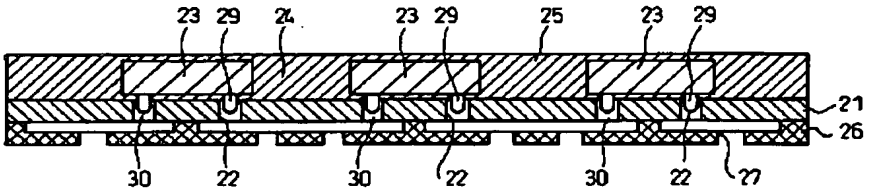
[Drawing 6]

図6



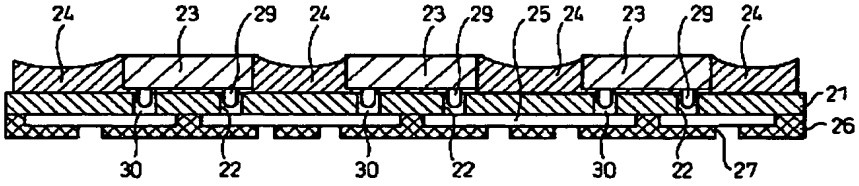
[Drawing 7]

図7



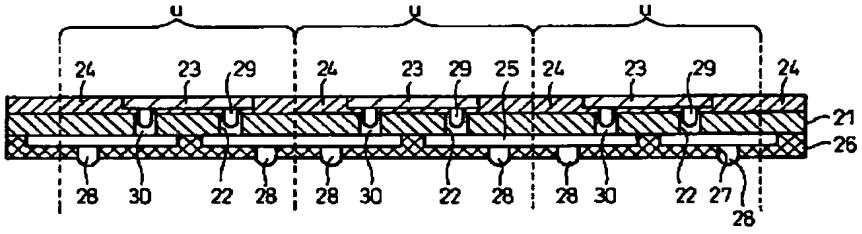
[Drawing 8]

図8



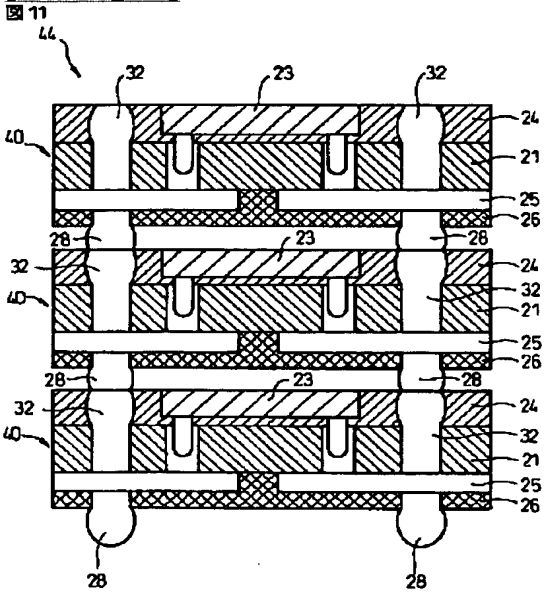
[Drawing 9]

図9



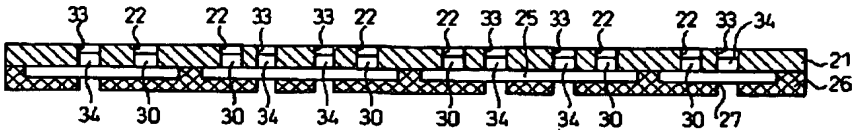
[Drawing 11]

図11



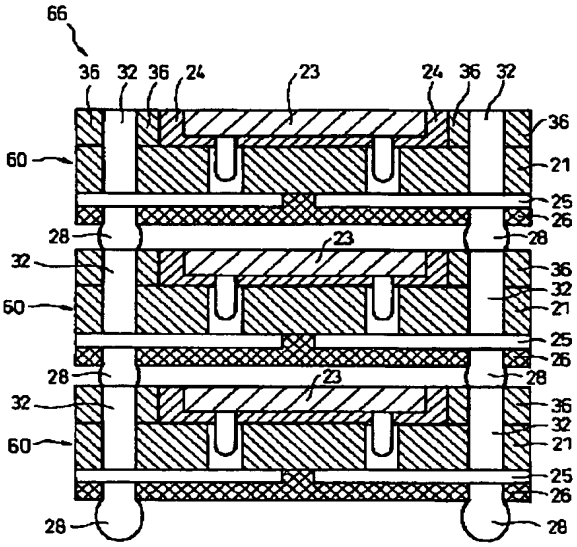
[Drawing 12]

図12



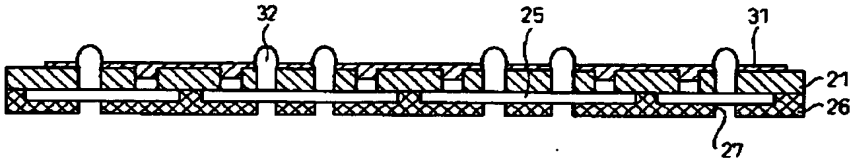
[Drawing 18]

図18



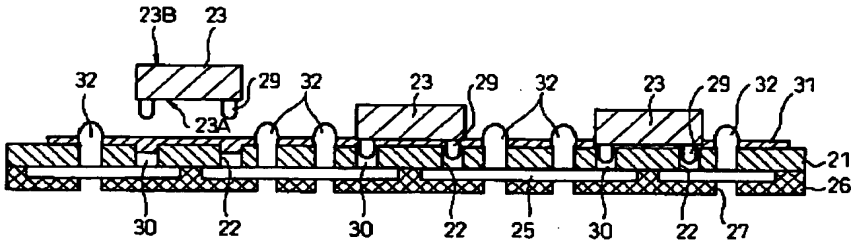
[Drawing 13]

図13



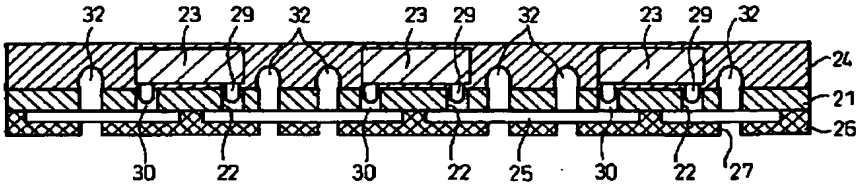
[Drawing 14]

図14



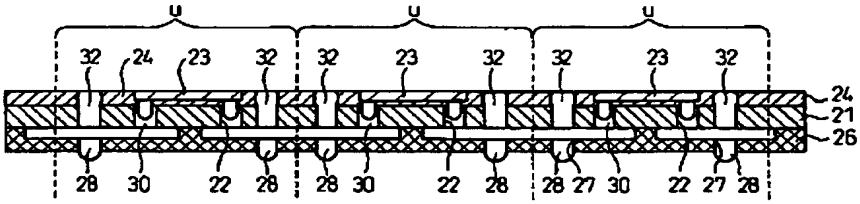
[Drawing 15]

図15



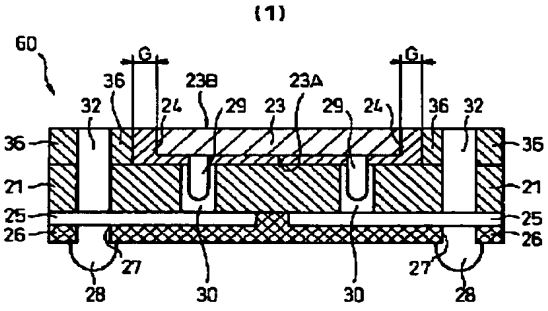
[Drawing 16]

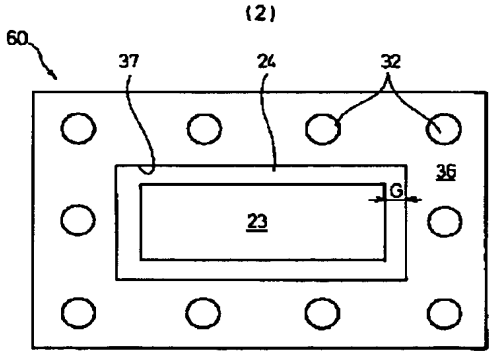
図16



[Drawing 17]

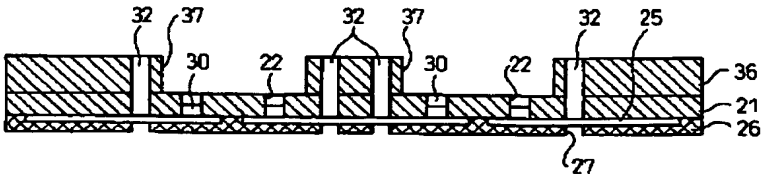
図17





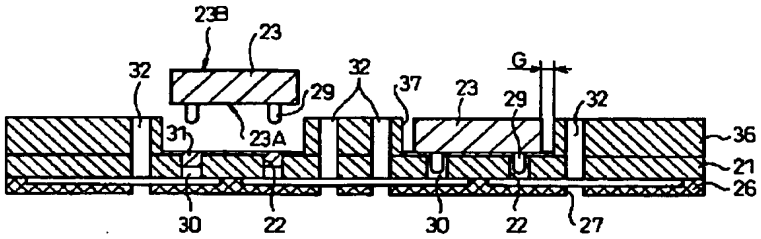
[Drawing 19]

図19



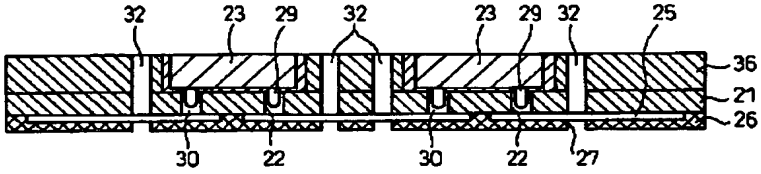
[Drawing 20]

図20



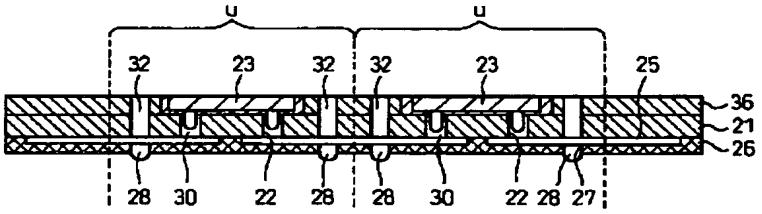
[Drawing 21]

図21



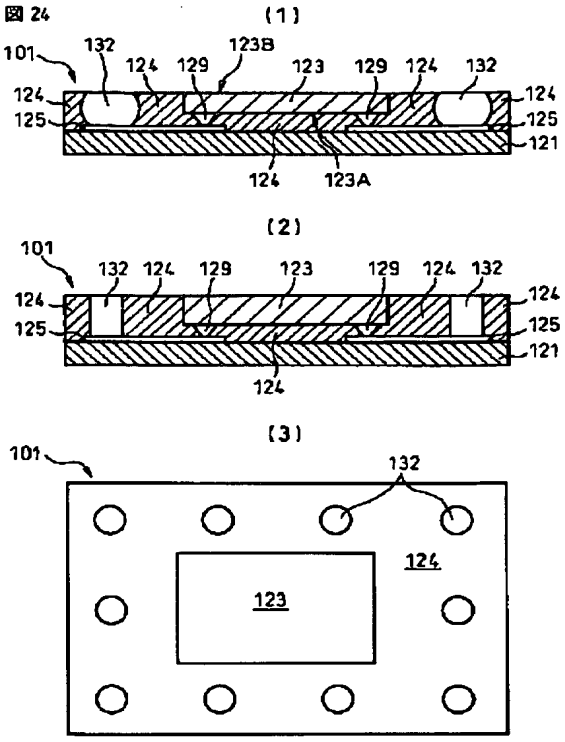
[Drawing 22]

図22



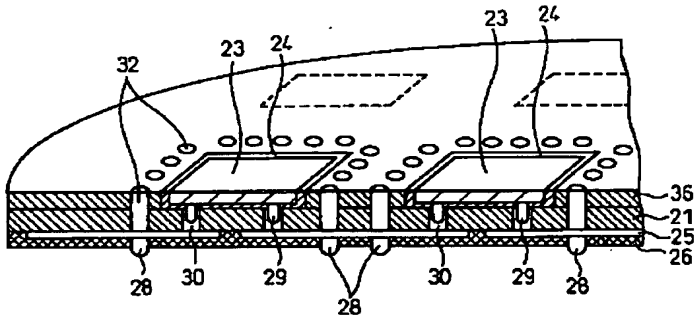
[Drawing 24]

図 24



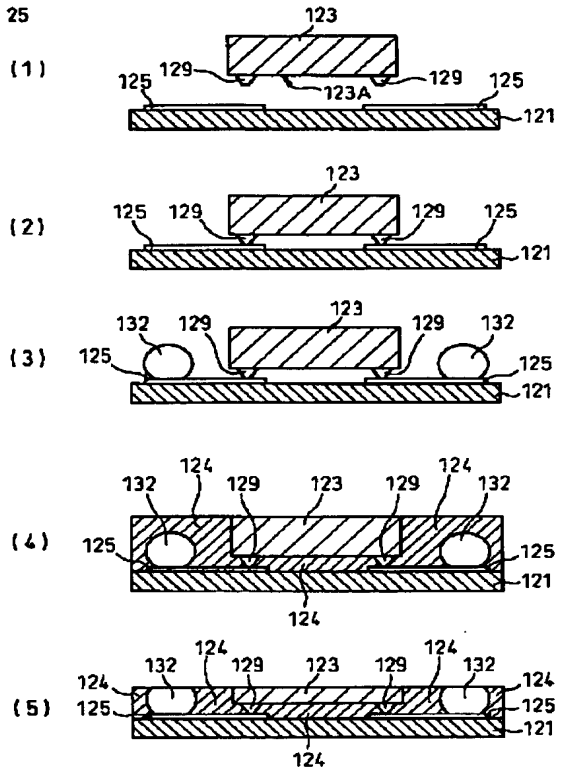
[Drawing 23]

図 23



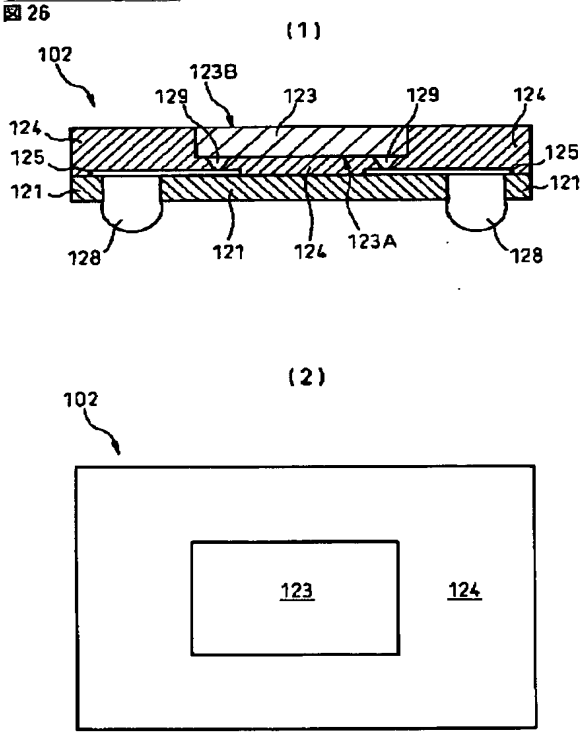
[Drawing 25]

図 25



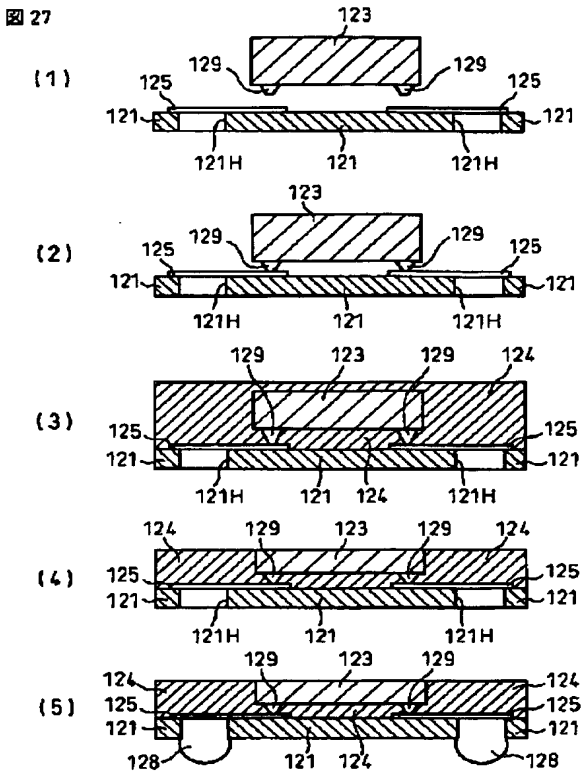
[Drawing 26]

図 26



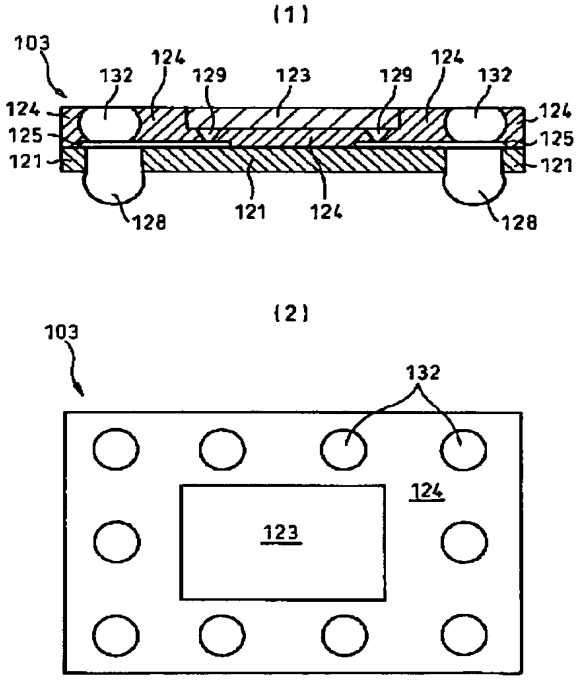
[Drawing 27]

図27



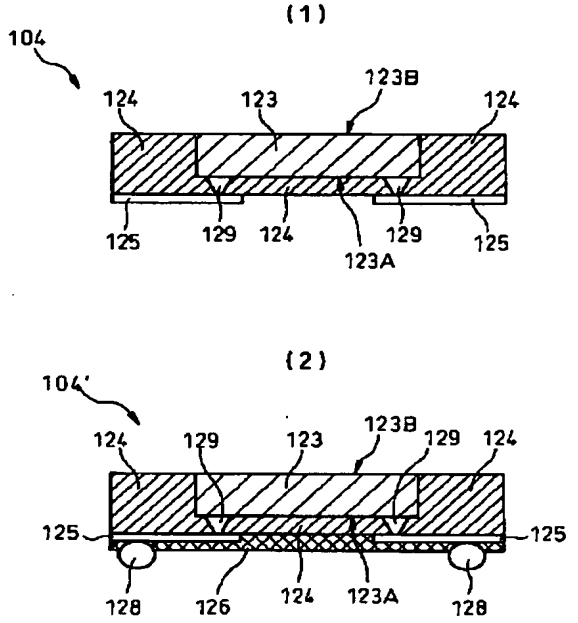
[Drawing 28]

図28



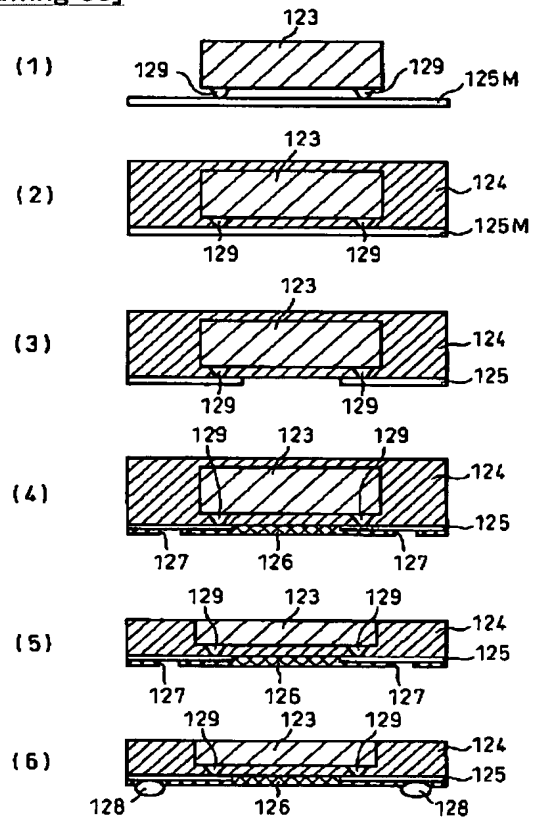
[Drawing 29]

図29



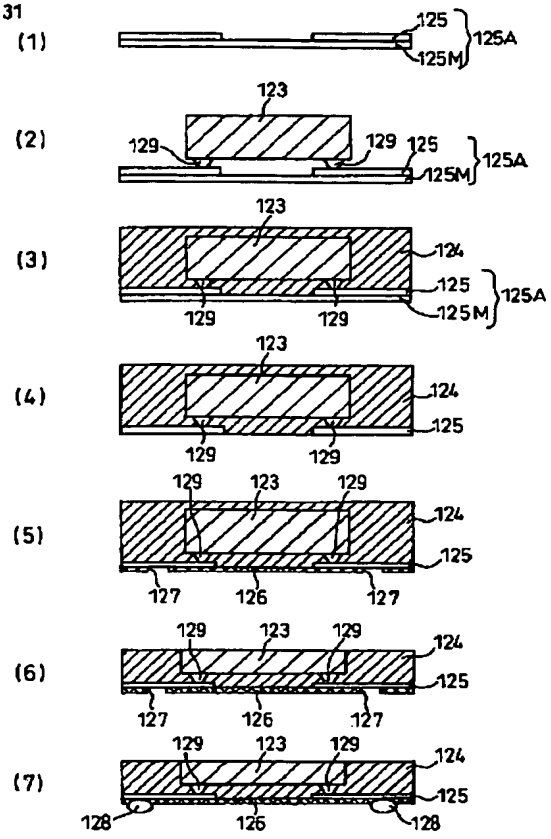
[Drawing 30]

図30



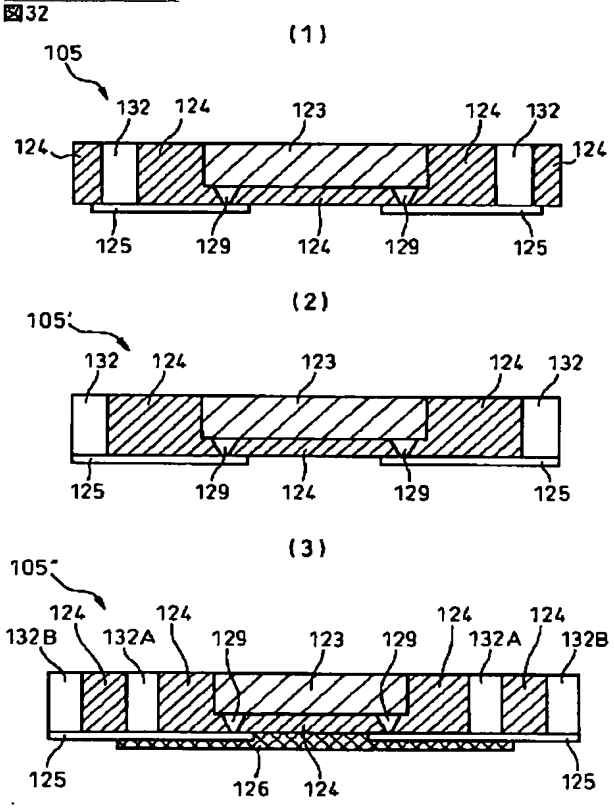
[Drawing 31]

図31



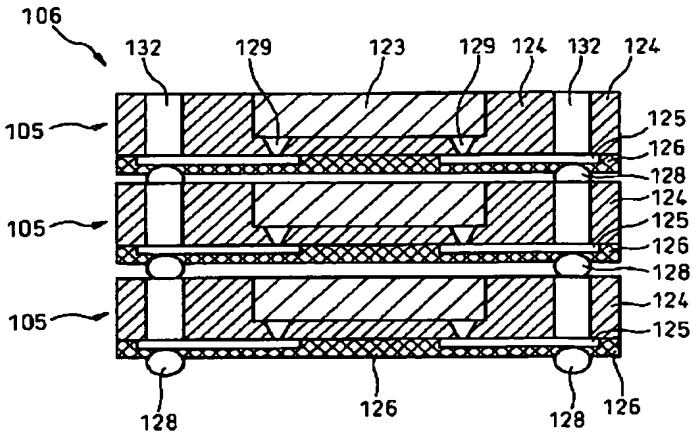
[Drawing 32]

図32



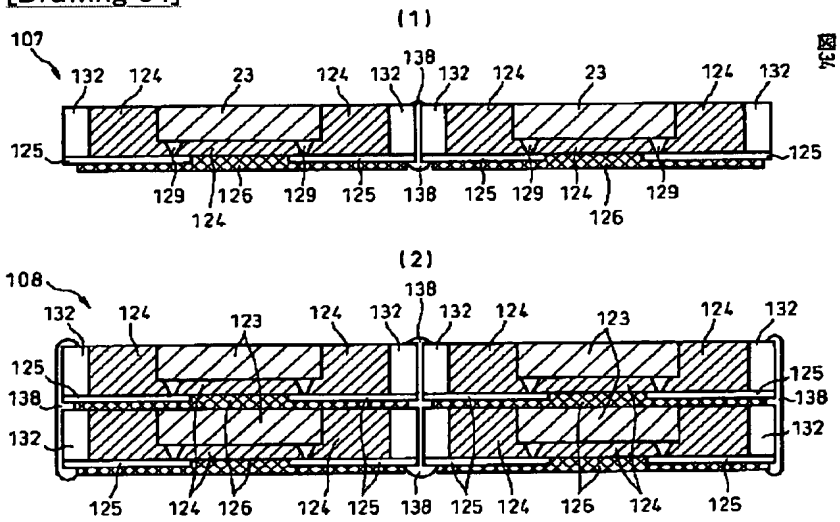
[Drawing 33]

図33



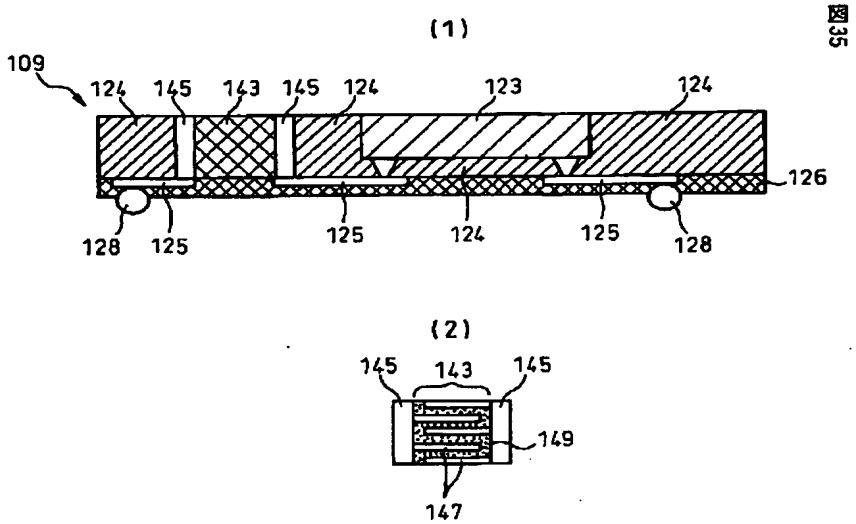
[Drawing 34]

図34



[Drawing 35]

図35



[Translation done.]

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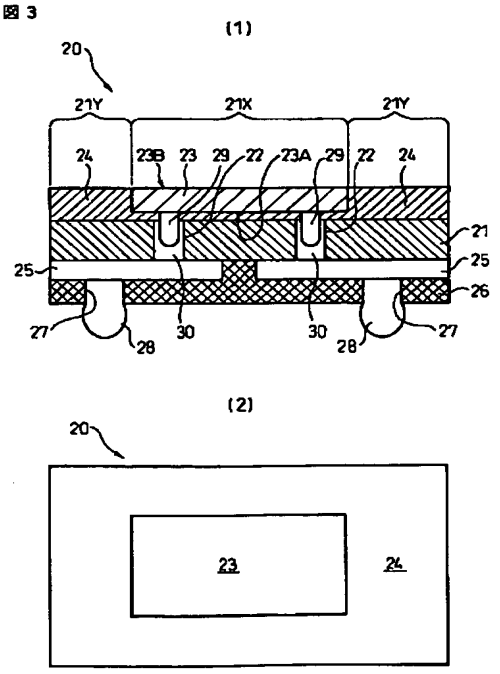
(54)【発明の名称】　半導体装置およびその製造方法

(57)【要約】
【課題】　取り付け高さを低減すると同時に均一化し、個々のチップ取り付けのための煩雑な工程を必要とせず、製造歩留りを向上し、チップの厚さばらつきに影響されずに半導体装置の高さを均一化し、電気試験の一括実行が可能な薄型半導体パッケージとしての半導体装置およびその製造方法を提供する。
【解決手段】　厚さ方向の貫通孔を有する絶縁性のテープ基材の上面に背面を上方に露出して半導体素子が搭載され、半導体素子の側面周囲は封止樹脂層で封止され、テープ基材の下面に形成された金属配線がテープ基材の貫通孔の底部を画定し、厚さ方向の貫通孔を有するソルダレジスト層が金属配線およびテープ基材の下面を覆い、半導体素子のアクティブ面から下方に延びた接続端子がテープ基材の貫通孔内に挿入され、導電性材料から成る充填材が接続端子とテープ基材の貫通孔の内壁との間隙を充填し接続端子と金属配線を電気的に接続している半導体装置。

図３



1

【特許請求の範囲】

【請求項１】　下記の部材：厚さ方向の貫通孔を有する絶縁性のテープ基材、

該テープ基材の上面に、背面を上方に露出し且つアクティブ面を下方に向けて搭載された半導体素子、

該半導体素子が搭載された領域以外の前記テープ基材上面に形成され、該半導体素子の側面周囲を封止する封止樹脂層、

前記テープ基材の下面に形成され且つ該テープ基材の貫通孔の下端を塞いで底部を画定する金属配線、

該金属配線および前記テープ基材の下面を覆い且つ厚さ方向の貫通孔を有するソルダレジスト層、

前記金属配線の下面から隆起し、前記ソルダレジスト層の貫通孔を充填して貫通し下方に突出した外部接続端子、

前記半導体素子のアクティブ面から下方に延びて、前記テープ基材の貫通孔内に挿入された接続端子、および該接続端子と前記テープ基材の貫通孔の内壁との間隙を充填し、該接続端子と前記金属配線とを電気的に接続する導電性材料から成る充填材、を含むことを特徴とする半導体装置。

【請求項２】　前記充填材が、低融点金属または導電性ペーストを用いて形成されていることを特徴とする請求項１記載の半導体装置。

【請求項３】　前記封止樹脂層および該封止樹脂層が形成されている領域の前記テープ基材を貫通し、上端が該封止樹脂層の上面に露出し、下端が前記金属配線層に電気的に接続している導体柱を更に含むことを特徴とする請求項１または２記載の半導体装置。

【請求項４】　前記封止樹脂層に代えて、前記半導体素子が搭載された領域以外の前記テープ基材上面に接合され該半導体素子の側面を間隙を介して取り囲む絶縁性の枠体と、該間隙内を充填して該半導体素子の側面周囲を封止する封止樹脂層とを含み、該枠体および該枠体が接合されている領域の前記テープ基材を貫通し、上端が該枠体の上面に露出し、下端が前記金属配線層に電気的に接続している導体柱を更に含むことを特徴とする請求項１記載の半導体装置。

【請求項５】　前記半導体素子のアクティブ面から下方に延びた接続端子が、金または銅から成るバンプであることを特徴とする請求項１から４までのいずれか１項記載の半導体装置。

【請求項６】　前記ソルダレジスト層の開口を充填して貫通する外部接続端子が、ペリフェラルまたはエリアアレイの形態で配置されていることを特徴とする請求項１から５までのいずれか１項記載の半導体装置。

【請求項７】　前記接続端子と前記テープ基材の貫通孔の内壁との間隙に、該貫通孔のほぼ上端の位置まで前記充填材が充填されていることを特徴とする請求項１から６までのいずれか１項記載の半導体装置。

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【請求項８】　前記封止樹脂層の上面と前記半導体素子の背面とが同一平面を成していることを特徴とする請求項１から７までのいずれか１項記載の半導体装置。

【請求項９】　請求項３または４記載の半導体装置が複数層に積層され、各層の半導体装置同士が、前記導体柱の上端と前記外部接続端子の下端とで相互に電気的に接続されていることを特徴とする素子積層型半導体装置。

【請求項１０】　請求項１から８までのいずれか１項記載の半導体装置の製造方法であって、

複数の半導体パッケージ単位を含み得る面積を有し、下面に前記金属配線層および前記ソルダレジスト層を備えた前記テープ基材および該ソルダレジスト層に各々厚さ方向の前記貫通孔を形成し、

該テープ基材の貫通孔に前記導電性材料を、該貫通孔を不完全に充填する量で充填し、

複数の半導体パッケージ単位を構成する必要個数の前記半導体素子の前記接続端子を上記テープ基材の対応する貫通孔に各々挿入して、該接続端子と該貫通孔の内壁との間隙を該貫通孔のほぼ上端まで該導電性材料により充填させると共に、該半導体素子を該テープ基材の上面に接合して搭載し、

該半導体素子が搭載された領域以外の該テープ基材の上面を覆い且つ少なくとも該半導体素子の側面周囲を封止する封止樹脂層を形成し、

その後、該封止樹脂層の上部および該半導体素子の背面側部分を研削および研磨して所定の厚さとし、

次いで、該テープ基材を前記半導体パッケージ単位に切り分けて個々の半導体装置とすることを特徴とする半導体装置の製造方法。

【請求項１１】　請求項３記載の半導体装置を製造するための請求項１０記載の方法であって、前記テープ基材に貫通孔を形成する際に請求項３記載の導体柱に対応する位置で該テープ基材を貫通する別の貫通孔を形成し、前記封止樹脂層を形成する前に該別の貫通孔を充填し且つ該テープ基材の上面から突き出た該導体柱を形成することを特徴とする半導体装置の製造方法。

【請求項１２】　請求項４記載の半導体装置を製造するための請求項１０記載の方法であって、請求項４記載の枠体の内壁を規定する開口を設けた絶縁性基材を前記テープ基材の上面に接合し、該テープ基材に前記貫通孔を形成する際に請求項４記載の導体柱に対応する位置で該絶縁性基材と該テープ基材とを貫通する別の貫通孔を形成し、前記半導体素子を搭載する前に該別の貫通孔を充填し且つ該絶縁性基材の上面に露出する該導体柱を形成し、該半導体素子を搭載した後に請求項４記載の間隙に前記封止樹脂層を形成することを特徴とする半導体装置の製造方法。

【請求項１３】　前記封止樹脂層を形成した後、前記研削および研磨の前または後に、電気的試験を行うことを特徴とする請求項１０から１２までのいずれか１項記載

の半導体装置の製造方法。

【請求項１４】　前記複数の半導体パッケージ単位を含み得るテープ基材が、直径２インチ以上１２インチ以下のディスク状であることを特徴とする請求項１０から１３までのいずれか１項記載の半導体装置の製造方法。

【請求項１５】　下記の部材①～④：

①上面に金属配線を有する絶縁性テープ基材、

②該テープ基材の上面に、背面を上方に露出し且つアクティブ面を下方に向けて搭載された半導体素子であって、該アクティブ面から下方へ突起した接続端子の下端が該金属配線の上面に接続している半導体素子、

③該テープ基材の上面に形成され、該半導体素子の側面周囲を封止し且つ該半導体素子の該アクティブ面と該テープ基材の上面との間隙を充填する封止樹脂層、および

④下記（Ａ）および（Ｂ）の少なくとも一方：

（Ａ）該金属配線の上面から上方に延びて該半導体素子の側面周囲の封止樹脂層を貫通し上端が上方に露出した導体柱、および

（Ｂ）該金属配線の下面から下方に延びて該テープ基材を貫通し下方に突出した外部接続端子、を含むことを特徴とする半導体装置。

【請求項１６】　前記封止樹脂層の上面と前記半導体素子の背面が同一平面を成していることを特徴とする請求項１５記載の半導体装置。

【請求項１７】　前記部材④として（Ａ）導体柱を備えた請求項１５記載の半導体装置の製造方法であって、

複数の半導体パッケージ単位を含み得る面積を有し、上面に前記金属配線を備えたテープ基材を準備し、

複数の半導体パッケージ単位を構成する必要個数の前記半導体素子の前記アクティブ面の前記接続端子を、上記テープ基材の上記金属配線の上面に接合することにより、該半導体素子を該テープ基材の上面に搭載し、

該金属配線の上面に下端が接合した導体柱を形成し、

該金属配線および該導体柱を含めて該半導体素子の側面周囲を封止し且つ該半導体素子の該アクティブ面と該テープ基材の上面との間隙を充填する封止樹脂層を形成し、

その後、該封止樹脂層の上部および該半導体素子の背面側部分を研削および研磨して所定の厚さとすると共に該導体柱の上端を上方に露出させ、

次いで、該テープ基材を前記半導体パッケージ単位に切り分けて個々の半導体装置とすることを特徴とする半導体装置の製造方法。

【請求項１８】　前記部材④として（Ｂ）外部接続端子を備えた請求項１５記載の半導体装置の製造方法であって、

複数の半導体パッケージ単位を含み得る面積を有し、上面に前記金属配線を備え、前記外部接続端子に対応する位置に厚さ方向の貫通孔を有し、該金属配線の下面が該貫通孔の上端を画定しているテープ基材を準備し、

複数の半導体パッケージ単位を構成する必要個数の前記半導体素子の前記アクティブ面の前記接続端子を、上記テープ基材の上記金属配線の上面に接合することにより、該半導体素子を該テープ基材の上面に搭載し、

該金属配線を含めて該半導体素子の側面周囲を封止し且つ該半導体素子の該アクティブ面と該テープ基材の上面との間隙を充填する封止樹脂層を形成し、

その後、下記工程（Ｓ１）および（Ｓ２）をこの順または逆順に行い：

（Ｓ１）該封止樹脂層の上部および該半導体素子の背面側部分を研削および研磨して所定の厚さとする工程、および

（Ｓ２）上記貫通孔の上端を画定する上記金属配線の下面から下方に延びて該貫通孔を充填して下方に突出した外部接続端子を形成する工程、

次いで、該テープ基材を前記半導体パッケージ単位に切り分けて個々の半導体装置とすることを特徴とする半導体装置の製造方法。

【請求項１９】　前記部材④として（Ａ）導体柱および（Ｂ）外部接続端子を備えた請求項１５記載の半導体装置の製造方法であって、

複数の半導体パッケージ単位を含み得る面積を有し、上面に前記金属配線を備え、前記外部接続端子に対応する位置に厚さ方向の貫通孔を有し、該金属配線の下面が該貫通孔の上端を画定しているテープ基材を準備し、

複数の半導体パッケージ単位を構成する必要個数の前記半導体素子の前記アクティブ面の前記接続端子を、上記テープ基材の上記金属配線の上面に接合することにより、該半導体素子を該テープ基材の上面に搭載し、

該金属配線の上面に下端が接合した導体柱を形成し、

該金属配線および該導体柱を含めて該半導体素子の側面周囲を封止し且つ該半導体素子の該アクティブ面と該テープ基材の上面との間隙を充填する封止樹脂層を形成し、

その後、下記工程（Ｓ１）および（Ｓ２）をこの順または逆順に行い：

（Ｓ１）該封止樹脂層の上部および該半導体素子の背面側部分を研削および研磨して所定の厚さとすると共に、前記導体柱の上端を上方に露出させる工程、および

（Ｓ２）上記貫通孔の上端を画定する上記金属配線の下面から下方に延びて該貫通孔を充填して下方に突出した外部接続端子を形成する工程、

次いで、該テープ基材を前記半導体パッケージ単位に切り分けて個々の半導体装置とすることを特徴とする半導体装置の製造方法。

【請求項２０】　下記の部材：所定厚さの樹脂体、

該樹脂体の内部に封止され、該樹脂体の上面に背面を露出し、アクティブ面を下方に向けた半導体素子、

該樹脂体の下面に形成された金属配線、および該半導体素子のアクティブ面から下方に延びて下端が該金属配線

の上面に接続している接続端子、を含むことを特徴とする半導体装置。

【請求項２１】　前記樹脂体の上面と前記半導体素子の背面が同一平面を成していることを特徴とする請求項２０記載の半導体装置。

【請求項２２】　前記金属配線を含めて前記樹脂体の下面全体を覆うソルダレジスト層と、該金属配線の下面に形成され上記ソルダレジスト層を貫通して下方に突き出ている接続バンプとを更に含むことを特徴とする請求項２０または２１記載の半導体装置。

【請求項２３】　前記金属配線の上面から前記樹脂体を貫通して上方に延び、上端が該樹脂体の上面に露出している複数の導体柱を更に含むことを特徴とする請求項２０から２２までのいずれか１項記載の半導体装置。

【請求項２４】　前記導体柱の側面が前記樹脂体の側面に露出していることを特徴とする請求項２３記載の半導体装置。

【請求項２５】　前記樹脂体の内部に封止され、該金属配線と直接接続しているキャパシタを更に含むことを特徴とする請求項２０から２４までのいずれか１項記載の半導体装置。

【請求項２６】　前記キャパシタが対向平板型であり、各平板の板面が前記樹脂体の厚さ方向に対して平行であることを特徴とする請求項２５記載の半導体装置。

【請求項２７】　前記樹脂体中に無機フィラーが分散していることを特徴とする請求項２０から２６までのいずれか１項記載の半導体装置。

【請求項２８】　請求項２３記載の半導体装置が複数層に積層され、各層の半導体装置同士が、前記導体柱の上端と前記金属配線の下面とで接続バンプを介して相互に電気的に接続されていることを特徴とする素子積層型半導体装置。

【請求項２９】　請求項２４記載の半導体装置が側面で相互に接続されており、側方に隣接する半導体装置同士が、前記樹脂体の側面に露出した導体柱の側面同士で相互に電気的に接続されていることを特徴とする素子並列型半導体装置。

【請求項３０】　請求項２４記載の半導体装置が複数層に積層され且つ側面で相互に接続されており、各層の半導体装置同士が、前記導体柱の上端と前記金属配線の下面とで接続バンプを介して相互に電気的に接続されており、且つ側方に隣接する半導体装置同士が、前記樹脂体の側面に露出した導体柱の側面同士で相互に電気的に接続されていることを特徴とする素子積層並列型半導体装置。

【請求項３１】　請求項２０から２５までのいずれか１項記載の半導体装置の製造方法であって、
複数の半導体パッケージ単位を含み得る面積を有する金属基板の上面に、前記半導体素子のアクティブ面を下方に向けて前記接続端子の先端を接合することにより、該

半導体素子を該金属基板に搭載し、
該金属基板の上面全体を樹脂で覆うことにより、内部に該半導体素子が封止され且つ下面に該金属基板が接合された樹脂体を形成し、
その後、下記工程（Ｓ１）および（Ｓ２）をこの順または逆順に行い：
（Ｓ１）該樹脂体の上部および該半導体素子の背面側部分を研削および研磨して所定の厚さとする工程、および
（Ｓ２）該金属基板をパターニングすることにより、上面が該接続端子の下端に接続された金属配線を、上記樹脂体の下面に形成する工程、
次いで、該樹脂体を前記半導体パッケージ単位に切り分けて個々の半導体装置とすることを特徴とする半導体装置の製造方法。

【請求項３２】　前記半導体素子を前記金属基板に搭載した後、前記樹脂体を形成する前に、該金属基板の上面に導体柱を形成する工程を更に含むことを特徴とする請求項３１記載の半導体装置の製造方法。

【請求項３３】　前記導体柱は、上端および／または側面が前記樹脂体から露出するように形成することを特徴とする請求項３２記載の半導体装置の製造方法。

【請求項３４】　請求項２０から２５までのいずれか１項記載の半導体装置を製造する方法であって、
複数の半導体パッケージ単位を含み得る面積を有する金属基板の上面に、該金属基板とは異種の金属から成る配線パターンを設けた複合金属板を作製する工程、
上記複合金属板の上記配線パターンの上面に、前記半導体素子のアクティブ面を下方に向けて前記接続端子の先端を接合することにより、該半導体素子を該複合金属板に搭載し、
該複合金属板の上面全体を樹脂で覆うことにより、内部に該半導体素子が封止され且つ下面に該複合金属板が接合された樹脂体を形成し、
その後、下記工程（Ｓ１）および（Ｓ２）をこの順または逆順で行い：
（Ｓ１）該樹脂体の上部および該半導体素子の背面側部分を研削および研磨して所定の厚さとする工程、および
（Ｓ２）該複合金属板の該金属基板をエッチングにより除去し、該配線パターンを残すことにより、上面が該接続端子の下端に接続された該配線パターンから成る金属配線を、上記樹脂体の下面に形成する工程、
次いで、該樹脂体を前記半導体パッケージ単位に切り分けて個々の半導体装置とすることを特徴とする半導体装置の製造方法。

【請求項３５】　前記半導体素子を前記複合金属板に搭載した後、前記樹脂体を形成する前に、該金属基板の上面に導体柱を形成する工程を更に含むことを特徴とする請求項３４記載の半導体装置の製造方法。

【請求項３６】　前記導体柱は、上端および／または側面が前記樹脂体から露出するように形成することを特徴

とする請求項３５記載の半導体装置の製造方法。

【請求項３７】　前記樹脂体の下面に前記金属配線を形成した後に、該金属配線を含めて該樹脂体の下面全体を覆うソルダレジスト層と、該金属配線の下面に形成され上記ソルダレジスト層を貫通して下方に突き出ている接続バンプとを形成する工程を更に含むことを特徴とする請求項３１または３４記載の半導体装置の製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、半導体装置およびその製造方法に関し、薄型パッケージとしての半導体装置およびその製造方法に関する。

【０００２】

【従来の技術】従来、半導体素子（ＬＳＩ等の半導体チップ）を搭載した薄型パッケージとしての半導体装置は、多ピン化、接続端子ピッチの縮小、装置全体の薄型化・小型化に最も良く適応しうるＴＣＰ（テープ・キャリア・パッケージ）が普及している。

【０００３】ＴＣＰは、ＴＡＢ（テープ・オートメイテド・ボンディング）方式により半導体素子を絶縁性のテープ状基材（通常は樹脂フィルム）に搭載して製造される。典型的には、先ず、所定パターンの開口部を設けた樹脂フィルムに銅箔を貼り付けた後、銅箔をエッチングによりパターニングして所定の銅リードを形成する。次に、半導体素子（半導体チップ）を樹脂フィルムの開口部内に位置決めして保持し、チップの複数の接続端子（一般には金バンプ）と樹脂フィルム上の対応する複数の銅リードとを接合した後、半導体チップと銅リードの一部を樹脂封止することにより、１つの半導体パッケージ単位が完成する。そして、樹脂フィルムを断続的に送りながら各開口部毎に上記の操作を繰り返すことにより、１つのフィルム上に多数の半導体パッケージ単位が形成される。最後に、フィルムの長手方向に沿って多数形成された各半導体パッケージ単位を相互間で切断分離することにより、個々の半導体パッケージとしての半導体装置が得られる。

【０００４】図１は、半導体チップとＴＣＰのリードを接続した後の従来の半導体装置を示す斜視図であり、個々のＴＣＰをテープから切断する前の状態を示す。ＴＣＰ１０は、樹脂フィルム（例えばポリイミド樹脂フィルム）１を基材として使用し、その上に銅箔のエッチングにより形成したリード２を有している。また、樹脂フィルム１の両側縁には、フィルム送りのためスプロケットホール３が開けられている。さらに、樹脂フィルム１の中央部には、図示されるように半導体チップ４を収容するための開口（一般に、「デバイスホール」と呼ばれる）５およびウインドウホール９も開けられている。

【０００５】半導体チップとパッケージのリードの接続の状態を、図１の半導体装置の中心部を拡大した図２の断面図に示す。半導体チップ４は、樹脂フィルム１のデバイスホール５に位置決めして配置された後、その電極上のバンプ（通常、金メッキからなる突起）６にリード２の先端が接合される。このリードの接合は、通常、専用のボンディングツールを使用して一括ボンディングで行われる。なお、銅からなるリード２の先端には、バンプ６との接合を助けるため、ボンディング工程に先がけて予め金メッキなどが施される。最後に、図１には示されていないが、半導体チップ４やリード６を周囲環境の湿度、汚染などから保護するため、両者を包み込むようにして樹脂７で封止する。封止用の樹脂７としては、例えば、エポキシ樹脂が使用される。

【０００６】しかし、上記従来の半導体装置には下記（ａ）～（ｅ）の問題があった。

（ａ）樹脂フィルムへの半導体チップの取り付け高さの低減に限界があるため、半導体装置の薄型化に限界がある。すなわち、半導体素子の固定は、樹脂フィルムの開口部内に梁状に細長く突き出た銅リードでなされるため、取り付け強度を確保するには、銅リード、その支持部材となる樹脂フィルム、そして装置全体にある程度以上の厚さが必要である。仮に樹脂封止部で補強させるとすると、広い範囲を厚く封止しなければならないが、広い範囲に渡って封止の完全性を確保することは困難であり、厚く封止すると薄型化に逆行する。

【０００７】（ｂ）半導体装置の薄型化に必要な薄く脆く反り易い半導体チップは、個々に特別なキャリアを要するなど取り扱いが非常に煩雑で多数の工程を要するだけでなく、製造歩留りの向上も困難である。

（ｃ）個々の半導体チップを１つ１つ樹脂フィルムの開口部に位置合わせして接合する必要があるので、多数の半導体パッケージを製造するには製造工程が煩雑で長くなる。

【０００８】（ｄ）半導体チップを複数層に積層した素子積層型半導体装置は、個々の半導体チップを樹脂フィルムの開口部に位置合わせ・ボンディングして取り付ける必要があるので、製造工程が更に煩雑で長くなる。

（ｅ）個々のチップに厚さのばらつきがある上、個々の取り付け高さにもばらつきがある結果、半導体装置に高さのばらつきが生ずるため、電気的試験を半導体パッケージ単位に切断分離する前に一括して行うことが困難である。

【０００９】

【発明が解決しようとする課題】本発明は、上記従来技術の問題を解消し、取り付け高さを低減すると同時に均一化し、個々のチップ取り付けのための煩雑な工程を必要とせず、製造歩留りを向上し、チップの厚さばらつきに影響されずに半導体装置の高さを均一化し、電気試験の一括実行が可能な薄型半導体パッケージとしての半導体装置およびその製造方法を提供することを目的とする。

【００１０】

【課題を解決するための手段および発明の実施の形態】上記の目的を達成するために、第１発明の半導体装置は、下記の部材：厚さ方向の貫通孔を有する絶縁性のテープ基材、該テープ基材の上面に、背面を上方に露出し且つアクティブ面を下方に向けて搭載された半導体素子、該半導体素子が搭載された領域以外の前記テープ基材上面に形成され、該半導体素子の側面周囲を封止する封止樹脂層、前記テープ基材の下面に形成され且つ該テープ基材の貫通孔の下端を塞いで底部を画定する金属配線、該金属配線および前記テープ基材の下面を覆い且つ厚さ方向の貫通孔を有するソルダレジスト層、前記金属配線の下面から隆起し、前記ソルダレジスト層の貫通孔を充填して貫通し下方に突出した外部接続端子、前記半導体素子のアクティブ面から下方に延びて、前記テープ基材の貫通孔内に挿入された接続端子、および該接続端子と前記テープ基材の貫通孔の内壁との間隙を充填し、該接続端子と該金属配線とを電気的に接続する導電性材料から成る充填材、を含むことを特徴とする。

【００１１】上記第１発明の半導体装置を製造する方法は、複数の半導体パッケージ単位を含み得る面積を有し、下面に前記金属配線層および前記ソルダレジスト層を備えた前記テープ基材および該ソルダレジスト層に各々厚さ方向の前記貫通孔を形成し、該テープ基材の貫通孔に前記導電性材料を、該貫通孔を不完全に充填する量で充填し、複数の半導体パッケージ単位を構成する必要個数の前記半導体素子の前記接続端子を上記テープ基材の対応する貫通孔に各々挿入して、該接続端子と該貫通孔の内壁との間隙を該貫通孔のほぼ上端まで該導電性材料により充填させると共に、該半導体素子を該テープ基材の上面に接合して搭載し、該半導体素子が搭載された領域以外の該テープ基材の上面を覆い且つ少なくとも該半導体素子の側面周囲を封止する封止樹脂層を形成し、その後、該封止樹脂層の上部および該半導体素子の背面側部分を研削および研磨して所定の厚さとし、次いで、該テープ基材を前記半導体パッケージ単位に切り分けて個々の半導体装置とすることを特徴とする。

【００１２】第１発明によれば、半導体素子のアクティブ面から下方に延びて、テープ基材の貫通孔内に挿入された接続端子、および接続端子とテープ基材の貫通孔の内壁との間隙を充填し、接続端子と金属配線とを電気的に接続する導電性材料から成る充填材を備えた構造としたことにより、半導体素子をアクティブ面で直接テープ基材と接合できると同時に、テープ基材の貫通孔に挿入した接続端子および間隙を充填する導電性材料から成る充填材により半導体素子を金属配線層に電気的に接続できるので、従来技術のように半導体素子をテープ基材の開口内にリードで固定する構造に比べて、取り付け強度を容易に確保して従来よりも薄型化することができる。

【００１３】第１発明によれば更に、テープ基材上に多数の半導体素子を固定し、半導体素子の側面周囲を樹脂封止した状態で、半導体素子の背面および封止樹脂層を上から研削および研磨して所定値まで高さを低減できるので、個々の半導体チップは薄くせずに厚い状態で取り扱うことができ、従来のように煩雑な工程も特別なキャリアも必要とせず、多数の半導体パッケージ単位をテープ基材に固定された一体として一括して製造でき、半導体パッケージとしての半導体装置の高さを薄くかつ均一に揃えることができ、電気的試験も一括して実行でき、製造工程を短縮し且つ製品歩留りを向上した上で、従来よりも薄型化することができる。

【００１４】第１発明の一形態による半導体装置は、①前記封止樹脂層および前記封止樹脂層が形成されている領域の前記テープ基材を貫通し、上端が該封止樹脂層の上面に露出し、下端が前記金属配線層に電気的に接続している導体柱を更に含む構造か、あるいは②前記封止樹脂層に代えて、前記半導体素子が搭載された領域以外の前記テープ基材上面に接合され該半導体素子の側面を間隙を介して取り囲む絶縁性の枠体と、該間隙内を充填して該半導体素子の側面周囲を封止する封止樹脂層とを含み、該枠体および該枠体が接合されている領域の該テープ基材を貫通し、上端が該枠体の上面に露出し、下端が前記金属配線層に電気的に接続している導体柱を更に含む構造である。

【００１５】上記①または②の構造は、積層型半導体装置の製造に適用すると特に有利である。これにより製造される第１発明の積層型半導体装置は、上記①または上記②の半導体装置が複数層に積層され、各層の半導体装置同士が、前記導体柱の上端と前記外部接続端子の下端とで相互に電気的に接続されている構造である。第１発明の半導体装置においては、前記半導体素子のアクティブ面から下方に延びた接続端子は、典型的には金または銅のバンプから成る。

【００１６】第１発明の半導体装置においては、前記ソルダレジスト層の開口を充填して貫通する外部接続端子は、半導体装置の用途あるいは顧客の要望に応じてペリフェラルまたはエリアアレイの形態で配置される。第１発明の半導体装置においては、前記接続端子と前記テープ基材の貫通孔の内壁との間隙を、該貫通孔のほぼ上端の位置まで前記充填材が充填していることが望ましい。すなわち、充填材の量は、後から挿入される半導体素子の接続端子との合計体積が、テープ基材の貫通孔（底部を金属配線が画定）の容積とほぼ等しくなるように設定する。これにより、接続端子と金属配線との接続が確実に成され、同時に、余分な導電性材料が貫通孔上端から溢れることが防止される。導電性材料としては、低融点金属または導電性ペーストを用いることができる。

【００１７】第１発明の製造方法においては、テープ基材上に形成された多数の半導体パッケージ単位の高さが均一に揃っているので、前記封止樹脂層を形成した後、前記研削および研磨の前または後に、容易に一括して電

気的試験を行うができる。第１発明の製造方法に用いるテープ基材は、前記複数の半導体パッケージ単位を含み得るサイズであって、直径２インチから１２インチまでのディスク状であることが望ましい。これにより、同サイズの半導体ウェハを処理する既存の研削機や切断機等の設備を用いることができるので、その分、新規設備のための費用を低減できる。

【００１８】第２発明の半導体装置は、下記の部材①～④：

①上面に金属配線を有する絶縁性テープ基材、

②該テープ基材の上面に、背面を上方に露出し且つアクティブ面を下方に向けて搭載された半導体素子であって、該アクティブ面から下方へ突起した接続端子の下端が該金属配線の上面に接続している半導体素子、

③該テープ基材の上面に形成され、該半導体素子の側面周囲を封止し且つ該半導体素子の該アクティブ面と該テープ基材の上面との間隙を充填する封止樹脂層、および

④下記（Ａ）および（Ｂ）の少なくとも一方：

（Ａ）該金属配線の上面から上方に延びて該半導体素子の側面周囲の封止樹脂層を貫通し上端が上方に露出した導体柱、および

（Ｂ）該金属配線の下面から下方に延びて該テープ基材を貫通し下端が下方に露出した外部接続端子、を含むことを特徴とする。典型的には、前記封止樹脂層の上面と前記半導体素子の背面が同一平面を成している。

【００１９】第２発明の半導体装置の製造方法は、部材④として（Ａ）導体柱と（Ｂ）外部接続端子の一方または両方を備える３つの場合に応じて、下記の（１）～（３）の形態をとる。

（１）部材④として（Ａ）導体柱を備えた第２発明の半導体装置の製造方法は、複数の半導体パッケージ単位を含み得る面積を有し、上面に前記金属配線を備えたテープ基材を準備し、複数の半導体パッケージ単位を構成する必要個数の前記半導体素子の前記アクティブ面の前記接続端子を、上記テープ基材の上記金属配線の上面に接合することにより、該半導体素子を該テープ基材の上面に搭載し、該金属配線の上面に下端が接合した導体柱を形成し、該金属配線および該導体柱を含めて該半導体素子の側面周囲を封止し且つ該半導体素子の該アクティブ面と該テープ基材の上面との間隙を充填する封止樹脂層を形成し、その後、該封止樹脂層の上部および該半導体素子の背面側部分を研削および研磨して所定の厚さとすると共に該導体柱の上端を上方に露出させ、次いで、該テープ基材を前記半導体パッケージ単位に切り分けて個々の半導体装置とすることを特徴とする。

【００２０】（２）部材④として（Ｂ）外部接続端子を備えた第２発明の半導体装置の製造方法は、複数の半導体パッケージ単位を含み得る面積を有し、上面に前記金属配線を備え、前記外部接続端子に対応する位置に厚さ方向の貫通孔を有し、該金属配線の下面が該貫通孔の上端を画定しているテープ基材を準備し、複数の半導体パッケージ単位を構成する必要個数の前記半導体素子の前記アクティブ面の前記接続端子を、上記テープ基材の上記金属配線の上面に接合することにより、該半導体素子を該テープ基材の上面に搭載し、該金属配線を含めて該半導体素子の側面周囲を封止し且つ該半導体素子の該アクティブ面と該テープ基材の上面との間隙を充填する封止樹脂層を形成し、その後、下記工程（Ｓ１）および（Ｓ２）をこの順または逆順に行い：

（Ｓ１）該封止樹脂層の上部および該半導体素子の背面側部分を研削および研磨して所定の厚さとする工程、および

（Ｓ２）上記貫通孔の上端を画定する上記金属配線の下面から下方に延びて該貫通孔を充填して下方に下端を露出した外部接続端子を形成する工程、次いで、該テープ基材を前記半導体パッケージ単位に切り分けて個々の半導体装置とすることを特徴とする。

【００２１】（３）部材④として（Ａ）導体柱および（Ｂ）外部接続端子を備えた第２発明の半導体装置の製造方法は、複数の半導体パッケージ単位を含み得る面積を有し、上面に前記金属配線を備え、前記外部接続端子に対応する位置に厚さ方向の貫通孔を有し、該金属配線の下面が該貫通孔の上端を画定しているテープ基材を準備し、複数の半導体パッケージ単位を構成する必要個数の前記半導体素子の前記アクティブ面の前記接続端子を、上記テープ基材の上記金属配線の上面に接合することにより、該半導体素子を該テープ基材の上面に搭載し、該金属配線の上面に下端が接合した導体柱を形成し、該金属配線および該導体柱を含めて該半導体素子の側面周囲を封止し且つ該半導体素子の該アクティブ面と該テープ基材の上面との間隙を充填する封止樹脂層を形成し、その後、下記工程（Ｓ１）および（Ｓ２）をこの順または逆順に行い：

（Ｓ１）該封止樹脂層の上部および該半導体素子の背面側部分を研削および研磨して所定の厚さとする工程、および

（Ｓ２）上記貫通孔の上端を画定する上記金属配線の下面から下方に延びて該貫通孔を充填して下方に下端を露出した外部接続端子を形成する工程、次いで、該テープ基材を前記半導体パッケージ単位に切り分けて個々の半導体装置とすることを特徴とする。

【００２２】第２発明によれば、半導体素子のアクティブ面から下方に突起した接続端子の下端が、テープ基材上面にある金属配線の上面に接続された構造としたことにより、第１発明のようにテープ基材の貫通孔内で充填材を介して接続端子と金属配線とが接続するよりも更に簡潔な構造とすることができるので、薄型半導体装置の生産性を更に高めることができる。

【００２３】第２発明においても、第１発明と同様に、テープ基材上に多数の半導体素子を固定し、半導体素子

の側面周囲を樹脂封止した状態で、半導体素子の背面および封止樹脂層を上から研削および研磨して所定値まで高さを低減できるので、個々の半導体チップは薄くせずに厚い状態で取り扱うことができ、従来のように煩雑な工程も特別なキャリアも必要とせず、多数の半導体パッケージ単位をテープ基材に固定された一体として一括して製造でき、半導体パッケージとしての半導体装置の高さを薄くかつ均一に揃えることができ、電気的試験も一括して実行でき、製造工程を短縮し且つ製品歩留りを向上した上で、従来よりも薄型化することができる。

【００２４】第３発明の半導体装置は、下記の部材：所定厚さの樹脂体、該樹脂体の内部に封止され、該樹脂体の上面に背面を露出し、アクティブ面を下方に向けた半導体素子、該樹脂体の下面に形成された金属配線、および該半導体素子のアクティブ面から下方に延びて下端が該金属配線の上面に接続している接続端子、を含むことを特徴とする。典型的には、前記樹脂体の上面と前記半導体素子の背面が同一平面を成している。

【００２５】第３発明の半導体装置を製造する第１の方法は、複数の半導体パッケージ単位を含み得る面積を有する金属基板の上面に、前記半導体素子のアクティブ面を下方に向けて前記接続端子の先端を接合することにより、該半導体素子を該金属基板に搭載し、該金属基板の上面全体を樹脂で覆うことにより、内部に該半導体素子が封止され且つ下面に該金属基板が接合された樹脂体を形成し、その後、下記工程（Ｓ１）および（Ｓ２）をこの順または逆順に行い：

（Ｓ１）該樹脂体の上部および該半導体素子の背面側部分を研削および研磨して所定の厚さとする工程、および

（Ｓ２）該金属基板をパターニングすることにより、上面が該接続端子の下端に接続された金属配線を、上記樹脂体の下面に形成する工程、次いで、該樹脂体を前記半導体パッケージ単位に切り分けて個々の半導体装置とすることを特徴とする。

【００２６】第３発明の半導体装置を製造する第２の方法は、複数の半導体パッケージ単位を含み得る面積を有する金属基板の上面に、該金属基板とは異種の金属から成る配線パターンを設けた複合金属板を作製する工程、上記複合金属板の上記配線パターンの上面に、前記半導体素子のアクティブ面を下方に向けて前記接続端子の先端を接合することにより、該半導体素子を該複合金属板に搭載し、該複合金属板の上面全体を樹脂で覆うことにより、内部に該半導体素子が封止され且つ下面に該複合金属板が接合された樹脂体を形成し、その後、下記工程（Ｓ１）および（Ｓ２）をこの順または逆順で行い：

（Ｓ１）該樹脂体の上部および該半導体素子の背面側部分を研削および研磨して所定の厚さとする工程、および

（Ｓ２）該複合金属板の該金属基板をエッチングにより除去し、該配線パターンを残すことにより、上面が該接続端子の下端に接続された該配線パターンから成る金属配線を、上記樹脂体の下面に形成する工程、次いで、該樹脂体を前記半導体パッケージ単位に切り分けて個々の半導体装置とすることを特徴とする。

【００２７】第３発明によれば、テープ基材を含まない構造としたことにより、第１発明および第２発明よりも更に薄型化できると同時に、部材数が少なく、より簡潔な構造であるため更に高い生産性を達成できる。第３発明においても、一体の樹脂体中に多数の半導体素子を封止し、半導体素子の背面および樹脂体を上から研削および研磨して所定値まで高さを低減できるので、個々の半導体チップは薄くせずに厚い状態で取り扱うことができ、従来のように煩雑な工程も特別なキャリアも必要とせず、多数の半導体パッケージ単位を樹脂体中に固定した一体として一括して製造でき、半導体パッケージとしての半導体装置の高さを薄くかつ均一に揃えることができ、電気的試験も一括して実行でき、製造工程を短縮し且つ製品歩留りを向上した上で、従来よりも薄型化することができる。

【００２８】一つの望ましい形態においては、前記金属配線を含めて前記樹脂体の下面全体を覆うソルダレジスト層と、該金属配線の下面に形成され上記ソルダレジスト層を貫通して下方に突き出ている接続バンプとを更に含む。

【００２９】別の望ましい形態においては、前記金属配線の上面から前記樹脂体を貫通して上方に延び、上端が該樹脂体の上面に露出している複数の導体柱を更に含む。この形態により、半導体装置が複数層に積層され、各層の半導体装置同士が、前記導体柱の上端と前記金属配線の下面とで上記接続バンプを介して相互に電気的に接続されている素子積層型半導体装置が容易に得られる。

【００３０】他の望ましい形態においては、前記導体柱の側面が前記樹脂体の側面に露出している。この形態により、半導体装置が側面で相互に接続されており、側方に隣接する半導体装置同士が、前記樹脂体の側面に露出した導体柱の側面同士で相互に電気的に接続されている素子並列型半導体装置が容易に得られる。

【００３１】更にもう一つの望ましい形態においては、前記導体柱の側面が前記樹脂体の側面に露出している。この形態により、半導体装置が複数層に積層され且つ側面で相互に接続されており、各層の半導体装置同士が、前記導体柱の上端と前記金属配線の下面とで接続バンプを介して相互に電気的に接続されており、且つ側方に隣接する半導体装置同士が、前記樹脂体の側面に露出した導体柱の側面同士で相互に電気的に接続されている素子積層並列型半導体装置が容易に得られる。

【００３２】上記各望ましい形態によれば、個々の半導体装置を検査し、良品のみを選択し積層および／または側方接続して素子積層型、素子並列型、素子積層並列型の半導体装置を製造することができるので、製品歩留り

を更に高めることができる。

【００３３】一形態においては、前記樹脂体の内部に封止され、該金属配線と直接接続しているキャパシタを更に含むことができる。望ましくは、前記キャパシタは対向平板型であり、各平板の板面が前記樹脂体の厚さ方向に対して垂直である。

【００３４】一形態においては、前記樹脂体中に無機フィラーが分散している。これにより樹脂体の熱膨脹係数および熱伝導率を所望値に調製することができる。

【００３５】

【実施例】以下、添付図面を参照し本発明を実施例により詳細に説明する。

〔実施例１〕図３（１）および（２）に、第１発明による半導体装置の一例を（１）断面図および（２）上面図でそれぞれ示す。

【００３６】図示した半導体装置２０は、厚さ方向の貫通孔２２を有する絶縁性のテープ基材２１の上面に、半導体素子２３が背面２３Ｂを上方に露出し且つアクティブ面２３Ａを下方に向けて接合されている。半導体素子２３が接合された領域２１Ｘ以外のテープ基材上面領域２１Ｙには、封止樹脂層２４が形成されおり、半導体素子２３の側面周囲を封止している。テープ基材２１の下面に形成された金属配線２５が、テープ基材２１の貫通孔２２の下端を塞いで底部を画定している。厚さ方向の貫通孔２７を有するソルダレジスト層２６が、金属配線２５およびテープ基材２１の下面を覆っている。金属配線２５の下面から隆起した外部接続端子２８が、ソルダレジスト層２６の貫通孔２７を充填して貫通し下方に突出している。半導体素子２３のアクティブ面２３Ａから下方に延びた接続端子２９が、テープ基材２１の貫通孔内に挿入されている。接続端子２９とテープ基材２１の貫通孔２２の内壁との間隙に充填された低融点金属の充填材３０によって、接続端子２９と金属配線２５とが電気的に接続されている。

【００３７】充填材３０としては、低融点金属に代えて導電ペーストを用いてもよい。導電ペーストとしては、ポリイミド樹脂やエポキシ樹脂中に銀または銅の粒子を分散させた銀ペーストまたは銅ペーストが一般的に用いられる。これらの導電ペーストをスクリーン印刷等により貫通孔内に充填する。図示の例では、半導体素子２３の背面と封止樹脂層２４の上面は同一平面上にあるが、封止樹脂層２４が半導体素子２３の側面周囲を封止している限り必ずしも同一平面でなくともよく、半導体素子２３の側面から離れた部位では封止樹脂層２４の高さが半導体素子２３の背面より低くてもよい。

【００３８】図３に示した第１発明の半導体装置の製造方法の一例を、図４～図９を参照して以下に説明する。図４に最初に準備する初期構造を示す。テープ基材２１は、複数の半導体パッケージ単位を含み得る面積を有し、下面に金属配線層２５およびソルダレジスト層２６を備えている。テープ基材２１としては、各種の有機材料あるいは高分子材料を用いることができるが、一般にポリイミドフィルム、ガラスやアラミド等の繊維で強化したエポキシフィルムあるいはＢＴ（ビスマレイミドトリアジン）フィルム、ＰＰＥ（ポリフェニレンエーテル）フィルム等の樹脂フィルムあるいは樹脂シートが適している。テープ基材２１の厚さは、基材として必要な強度および剛性が確保される限り薄い方が半導体装置の薄型化にとっては望ましく、一般には２５μｍ～１００μｍの範囲、特に７５μｍ前後が用いられる。

【００３９】テープ基材２１にパンチング等により貫通孔２２を形成した後、片面に金属配線層２５を形成するための銅箔を貼り付ける。あるいは、テープ基材２１と銅箔とが一体化された銅箔付テープを用い、テープ基材２１部分にレーザ加工を施すことにより、テープ基材２１を貫通し銅箔を底部とする孔を形成してもよい。銅箔付テープは、銅箔にポリイミド等の樹脂の塗布により絶縁層を形成したものである。

【００４０】次に、テープ基材２１の貫通孔２２（金属配線層２５により底部が画定）に、低融点金属の充填材３０を不完全に充填する。すなわち、後工程で半導体素子２１の接続端子２９を挿入したときに、充填材３０が接続端子２９と貫通孔２２の内壁との間隙を貫通孔２２のほぼ上端まで満たすような充填量とする。充填材３０の低融点金属としては、銀－錫合金（Ａｇ－Ｓｎ）、鉛－錫合金（Ｐｂ－Ｓｎ）、銀－錫－銅合金（Ａｇ－Ｓｎ－Ｃｕ）、これらにビスマス（Ｂｉ）やアンチモン（Ｓｂ）を含む合金等を用いることができる。充填は、銅箔を給電層として用いた電解めっきにより行うことが望ましいが、はんだペーストのスクリーン印刷によって行うこともできる。

【００４１】次いで、上記の銅箔をエッチングによりパターニングして金属配線層２５を形成する。金属配線層２５の形成後に、貫通孔２７を有するソルダレジスト層２６を形成する。貫通孔２７を有するソルダレジスト層２６の形成は、一般的には感光性レジストの塗布、露光、現像により行う。外部接続端子の個数（貫通孔２７の個数）が少なく、外部接続端子間のピッチが十分大きい場合には、樹脂のスクリーン印刷によって行うことができる。ソルダレジスト層２６の貫通孔２７は、製造する半導体装置２０の用途に応じてペリフェラルまたはエリアアレイ状に形成する。

【００４２】次に、図５に示すように、テープ基材２１の上面に液状あるいは半硬化状態の樹脂から成る絶縁性コーティング３１を塗布する。半硬化状態の絶縁性コーティング３１は半導体素子を接着する作用がある。次いで、図６に示すように、硬化前のコーティング３１の上に半導体素子２３を配置して接合する。すなわち、複数の半導体パッケージ単位を構成する必要個数の半導体素子２３の接続端子２９をテープ基材２１の対応する貫通

孔２２に各々挿入して、接続端子２９と貫通孔２２の内壁との間隙を貫通孔２２のほぼ上端まで低融点金属３０により充填させると共に、半導体素子２３をテープ基材２１の上面に接合して搭載する。これは、半導体素子２３を低融点金属３０の融点近傍の温度に加熱して、接続端子２９を貫通孔２２内の低融点金属３０中に押し込むことにより行う。

【００４３】半導体素子２３の接続端子２９は、金または銅のバンプとして形成することが望ましい。接続端子２９が周縁領域に配置されている半導体素子２３の場合には、一般にワイヤボンディング法を利用したスタッドバンプとして接続端子２９を形成する。接続端子２９が中央部のアクティブ領域に配置されている半導体素子２３の場合には、スタッドバンプ形成による機械的衝撃を避ける観点から、めっき法により接続端子２９を形成することが望ましい。めっき法は、半導体素子上に再配線部を伴いエリアアレイ状にバンプを形成する場合に特に有利である。スタッドバンプは金で形成することが望ましく、めっきバンプは保護めっき層を備えた銅ポストとして形成することが望ましい。

【００４４】接続端子すなわちバンプ２９のサイズは、半導体装置２０の設計厚さに応じて任意に設定できる。一例においては、バンプ２９は底部の直径が７０μｍ、高さ３０～６０μｍである。その場合、バンプ２９の形成における位置決め精度を考慮すると、バンプ２９が挿入されるテープ基材２１の貫通孔２２は直径９０～１５０μｍ程度の範囲が適当である。

【００４５】次に、図７に示すように、半導体素子２３が搭載された領域以外のテープ基材２１の上面を覆い且つ少なくとも半導体素子２３の側面周囲を封止する封止樹脂層２４を形成する。なお、図７～図９においては、非常に薄い絶縁性コーティング３１は封止樹脂層２４と一体として図示し、別個の図示は省略した。図７には、封止樹脂層２４は半導体素子２３も覆い、全体がほぼ同一厚さに形成されている態様を示した。ただし別の態様として、図８に示したように、この工程段階において封止樹脂層２４は半導体素子２３を必ずしも覆う必要はなく、半導体素子２３の側面との接触部は封止樹脂層２４の厚さを半導体素子２３の高さと同等とし、半導体素子２３から離れた領域ではこれより薄くてもよい。すなわち、この工程段階で形成する封止樹脂層２４の厚さは、次工程で行う研削および研磨後に半導体素子２３の側面周囲を完全に封止できる厚さで残るように設定すればよい。

【００４６】次に、図９に示すように、封止樹脂層２４の上部および半導体素子２３の背面２３Ｂ側部分を研削および研磨して所定の厚さとする。これにより、例えば図７あるいは図８の状態で５００μｍ程度であった半導体素子２３を５０～１００μｍ程度に薄くすることができる。その結果、半導体装置２０は、１２０～３００μｍ程度に薄くできる。これは、従来最も多用されているＴＳＯＰ（Thin-Small-Outline Package）の厚さ１２００μｍ程度と比較すると、１／４以下の厚さである。

【００４７】研削および研磨後に、ソルダレジスト層２６の貫通孔２７内に、ソルダレジスト層２６の下面から突き出た外部接続端子２８を形成する。これは、はんだボールの搭載またははんだペーストのスクリーン印刷の後、リフローすることにより行う。最後に、図９に破線で示した各位置で半導体パッケージ単位ｕに切り分けることにより、個々の半導体装置２０（図３）が得られる。

【００４８】〔実施例２〕図１０（１）および（２）に、第１発明による半導体装置の他の例を（１）断面図および（２）上面図でそれぞれ示す。図３に示す実施例１の構造と対応する部分には図３中と同じ参照番号を付した。図示した半導体装置４０は、図３に示した構造に加えて、低融点金属の導体（導体柱）３２を更に含む。導体３２は、半導体素子２３の側面周囲を封止する封止樹脂層２４および封止樹脂層２４が形成されている領域のテープ基材２１を貫通し、上端が封止樹脂層２４の上面に露出し、下端が金属配線層２５に電気的に接続している。

【００４９】図１０の半導体装置４０は、図１１に示したように複数層積層して薄型の積層型半導体装置４４を有利に形成できる。すなわち、下層の半導体装置４０の低融点金属の導体３２の上端と、上層の半導体装置４０の外部接続端子２８の下端とを接続することにより、積層構造全体として複数（この例では３個）の半導体素子２３を含む一体の回路から成る１つの半導体装置４４を構成する。半導体装置４０の積層は、下記のようにして行うことができる。

【００５０】すなわち、半導体装置の外形を有する治具（外形ガイド）で複数の半導体装置を位置決めしながら積層し、積層方向に適当な荷重を負荷した状態で一括してリフローすることにより積層型半導体装置が得られる。あるいは、個々の半導体装置に設けたガイド孔にピンを通して位置決めしながら複数の半導体装置を積層し、積層方向に適当な荷重を負荷した状態で一括してリフローしてもよい。

【００５１】図１０に示した第１発明の半導体装置の製造方法の一例を、図１２～１６を参照して以下に説明する。図４～図９に示す実施例１の構造に対応する部分には図４～図９中と同じ参照番号を付した。図１２に示した初期構造は、テープ基材２１に貫通孔２２の他に貫通孔３３が形成されている以外は、図４に示した実施例１の初期構造と同様である。貫通孔２２は実施例１と同様に半導体素子２３の接続端子２９に対応する位置に設けてあり、貫通孔３３は半導体素子２３の側面周囲を封止する封止樹脂層２４の形成領域内に設けてある。通常、貫通孔３３は貫通孔２２に対して直径が数倍の大きさで

ある。例えば、貫通孔２２が直径２５～１００μm程度であるのに対して、貫通孔３３は直径５００μm程度である。金属配線層２５によって底面を画定された貫通孔３３内に、少量のフラックス３４を配置する。図１２に示した初期構造の他の部分については、実施例１と同様の処理によって形成する。

【００５２】次に、図１３に示したように、貫通孔３３内に、封止樹脂層２４の上面から突き出た低融点金属の導体３２を形成する。これは、貫通孔３３内のフラックス３４上に、低融点金属の球（例えば、はんだボール）を載せ、リフローすることにより行う。その後、実施例１と同様にして絶縁性のコーティング３１を形成する。

【００５３】次に、図１４に示すように、実施例１と同様にして、硬化前のコーティング３１の上に半導体素子２３を配置して接合する。これに伴い、半導体素子２３のアクティグ面２３Ａから隆起した接続端子２９が、テープ基材２１の貫通孔２２内に挿入され、低融点金属３０の中に押し込まれる。次に、図１５に示すように、半導体素子２３が搭載された領域以外のテープ基材２１の上面を覆い且つ少なくとも半導体素子２３の側面周囲を封止する封止樹脂層２４を形成する。図１５～図１６において、絶縁性のコーティング３１は図示を省略した。

【００５４】図１５には、封止樹脂層２４は半導体素子２３も覆い、全体がほぼ同一厚さに形成されている態様を示した。ただし、実施例１について図８に示したように、この工程段階においては封止樹脂層２４は半導体素子２３を必ずしも覆う必要はなく、半導体素子２３の側面との接触部は封止樹脂層２４の厚さを半導体素子２３の高さと同等とし、半導体素子２３から離れた領域ではこれより薄くてもよい。すなわち、この工程段階で形成する封止樹脂層２４の厚さは、次工程で行う研削および研磨後に半導体素子２３の側面周囲を完全に封止できる厚さで残るように設定すればよい。

【００５５】次に、図１６に示すように、封止樹脂層２４の上部、導体３２の頂部および半導体素子２３の背面２３Ｂ側部分を研削および研磨して所定の厚さとする。研削および研磨後に、ソルダレジスト層２６の貫通孔２７内に、実施例１と同様にして外部接続端子２８を形成する。最後に、図１６に破線で示した各位置で半導体パッケージ単位ｕに切り分けることにより、個々の半導体装置４０（図１０）が得られる。

【００５６】〔実施例３〕図１７（１）および（２）に、第１発明による半導体装置のもう一つの例を（１）断面図および（２）上面図でそれぞれ示す。図３に示す実施例１の構造と対応する部分には図３中と同じ参照番号を付した。図示した半導体装置６０は、図３に示した構造における封止樹脂層２４に代えて、半導体素子２３が搭載された領域以外のテープ基材２１上面に接合され半導体素子２３の側面を間隙Ｇを介して取り囲む絶縁性の枠体３６と、間隙Ｇ内を充填して半導体素子２３の側面周囲を封止する封止樹脂層２４とを含み、枠体３６および枠体３６が接合されている領域のテープ基材２１を貫通し、上端が枠体３６の上面に露出し、下端が金属配線層２５に電気的に接続している低融点金属の柱状の導体（導体柱）３２を更に含む構造である。

【００５７】図１７の半導体装置６０は、図１８に示したように複数層積層して薄型の積層型半導体装置６６を有利に形成できる。すなわち、下層の半導体装置６０の低融点金属の柱状の導体３２の上端と、上層の半導体装置６０の外部接続端子２８の下端とを接続することにより、積層構造全体として複数（この例では３個）の半導体素子２３を含む一体の回路から成る１つの半導体装置６６を構成する。半導体装置６０の積層は、実施例２と同様にして行うことができる。

【００５８】図１７に示した第１発明の半導体装置６０の製造方法の一例を、図１９～２２を参照して以下に説明する。図４～図９に示す実施例１の構造に対応する部分には図４～図９中と同じ参照番号を付した。図１９に示した初期構造は、図４に示した構造に加えて、テープ基材２１の上面に、半導体素子２３を搭載する領域に開口３７を有する絶縁性基材３６が接合されており、テープ基材２１および絶縁性基材３６を貫通して柱状の導体３２が形成されている。開口３７は、図１７（２）に示したように、間隙Ｇを介して半導体素子２３を収容し得る形状および寸法になっている。テープ基材２１の貫通孔２２は実施例１と同様に半導体素子の接続端子２９に対応する位置に設けてある。

【００５９】絶縁性基材３６はテープ基材２１と同じ外形のテープ状であり、パンチング等により開口３７を形成した後に、テープ基材２１の上面に接合される。その後、柱状導体３２を形成する位置に、レーザー加工により絶縁性基材３６およびテープ基材２１を貫通する貫通孔を開口する。次いで、金属配線層２５にパターニングする前の銅箔を給電層として用いた孔埋めめっきにより、柱状導体３２を形成する。図１９の初期構造の他の部分については、実施例１と同様の処理により形成する。通常、柱状導体３２は貫通孔２２に対して直径が数倍の大きさである。例えば、貫通孔２２が直径２５～１００μm程度であるのに対して、柱状導体３２は直径５００μm程度である。次に、図２０に示すように、開口３７内に露出したテープ基材２１の上面に絶縁性のコーティング３１を形成した後、実施例１と同様にして、硬化前のコーティング３１の上に半導体素子２３を配置して接合する。これに伴い、半導体素子２３のアクティグ面２３Ａから隆起した接続端子２９が、テープ基材２１の貫通孔２２内に挿入され、低融点金属３０の中に押し込まれる。

【００６０】次に、図２１に示すように、半導体素子２３と絶縁性基材３６の開口３７との間隙Ｇを、封止樹脂層２４で封止する。これにより半導体素子２３の側面周

囲が封止される。図２１～図２２において、絶縁性のコーティング３１は図示を省略した。次に、図２２に示すように、絶縁性基材３６の上部、封止樹脂層２４の上部、導体３２の頂部および半導体素子２３の背面２３Ｂ側部分を研削および研磨して所定の厚さとする。

【００６１】研削および研磨後に、ソルダレジスト層２６の貫通孔２７内に、実施例１と同様にして外部接続端子２８を形成する。最後に、図２２に破線で示した各位置で半導体パッケージ単位ｕに切り分けることにより、個々の半導体装置６０（図１７）が得られる。

〔実施例４〕図２３に、テープ基材２１を含む初期構造として、直径2インチから１２インチまでのディスク状のものを用いて製造した、切り分け前の構造を示す。このような形状および寸法の初期構造を用いることにより、同サイズの半導体ウェハを処理する既存の研削機や切断機等の設備を用いることができるので、その分、新規設備のための費用を低減できる。図２３には、実施例３の構造の半導体素子を製造する場合を示したが、もちろん実施例１および実施例２の場合にも同様に適用できる。

【００６２】〔実施例５〕図２４（１）、（２）および（３）に、第２発明による半導体装置の一例を（１）断面図、（２）断面図および（３）上面図でそれぞれ示す。実施例１～４の構造と対応する部分には、これら実施例における参照番号に１００を加算した参照番号を付した（以降の実施例においても同様）。図示した半導体装置１０１は、絶縁性テープ基材１２１の上面に、金属配線１２５が形成されており、半導体素子１２３が背面１２３Ｂを上方に露出しアクティブ面１２３Ａを下方に向けて搭載されている。半導体素子１２３のアクティブ面１２３Ａから下方へ突起した接続端子１２９の下端が金属配線１２５の上面に接続してる。テープ基材１２１の上面に形成された封止樹脂層１２４が、半導体素子１２３の側面周囲を封止し且つ半導体素子１２３のアクティブ面１２３Ａとテープ基材１２１の上面との間隙を充填している。

【００６３】導体柱１３２が、金属配線１２５の上面から上方に延びて半導体素子１２３の側面周囲の封止樹脂層１２４を貫通し、上端を上方に露出している。導体柱１３２は、図２４（１）に示したようにほぼボール状（より正確にはエンタシス状）であってもよいし、図２４（２）に示したように直棒状であってもよい。導体柱１３２は、銅またはニッケル等の金属の柱またはボールであり、望ましくははんだ等の低融点金属のボールである。このはんだとしては、銀ー錫合金（Ａｇ－Ｓｎ）、鉛ー錫合金（Ｐｂ－Ｓｎ）、銀ー錫ー銅合金（Ａｇ－Ｓｎ－Ｃｕ）、これらにビスマス（Ｂｉ）やアンチモン（Ｓｂ）を含むはんだを用いることができる。

【００６４】図２５を参照して、図２４に示した半導体装置１０１の製造方法を説明する。本実施例は、実施例１～４と同様に多数の半導体パッケージ単位について一括して製造する場合に適用できるが、以下においては、説明を簡潔にするために、単一の半導体パッケージ単位について製造する形で説明する。先ず、図２５（１）に示すように、アクティブ面１２３Ａに接続端子１２９を備えた半導体素子１２３と、上面に金属配線１２５を備えたテープ基材１２１を準備する。接続端子１２９の形成方法、テープ基材１２１の材料構成、金属配線１２５の形成方法は、実施例１と同様である。

【００６５】次に、図２５（２）に示すように、半導体素子１２３のアクティブ面１２３Ａの接続端子１２９を、テープ基材１２１の金属配線１２５の上面に接合することにより、半導体素子１２３をテープ基材１２１の上面に搭載する。この接合（搭載）は下記のようにして行うことができる。予め、めっき等により金属配線１２５の所定位置に形成した金属（はんだ）層に接続端子１２９を加熱圧接するか、または、金属配線１２５上の金めっき上に金バンプから成る接続端子１２９を載せて超音波印加により直接接合または異方導電性フィルムかペーストを介して接合する。

【００６６】次に、図２５（３）に示すように、金属配線１２５の上面に下端が接合した導体柱１３２を形成する。図示の例では、導体柱１３２は図２４（２）に示したほぼボール状（より正確にはエンタシス状）であり、はんだボールである。はんだボールを用いた導体柱１３２の形成は、金属配線１２５上面の所定箇所に、はんだボールを搭載するか、またははんだペーストをスクリーン印刷した後に、リフローすることにより行うことができる。導体柱１３２は図２４（２）に示した直棒状であってもよい。直棒状の導体柱１３２の形成は下記のようにして行うことができる。表面にはんだめっき、錫（Ｓｎ）めっき、インジウム（Ｉｎ）めっき等を施した金属、好ましくは銅、の棒状体を、金属配線１２５上面の所定箇所に加熱加圧により接合するか、または、予め金属配線１２５上面の所定箇所にはんだ等のめっきを施した上に上記棒状体を搭載し、リフローする。

【００６７】次に、図２５（４）に示すように、封止樹脂層１２４を形成する。封止樹脂層１２４は、金属配線１２５および導体柱１３２を含めて半導体素子１２３の側面周囲を封止し且つ半導体素子１２３のアクティブ面１２３Ａとテープ基材１２１の上面との間隙を充填する。封止樹脂層１２４の形成は、モールディングまたはポッティングにより行うことができる。

【００６８】次に、図２５（５）に示すように、封止樹脂層１２４の上部および半導体素子１２３の背面側部分を研削および研磨して所定厚さとし、導体柱１３２の上端を上方に露出させる。図２５（４）の工程で、封止樹脂層１２４の上面は半導体素子１２３の上面（背面）と同一平面としてあるが、必ずしもその必要はなく、図２５（５）の研削・研磨により半導体素子１２３を含めた

全体を所定厚さとしたときに導体柱１３２の上端が上方に露出するように封止樹脂層１２４の厚さを設定すればよい。

【００６９】図２５には単一の半導体パッケージ単位についてのみ示したが、実際には複数の半導体素子パッケージ単位を含み得る面積のテープ基材１２１を用いて、図２５（１）～（５）の工程を行うことにより、多数の半導体パッケージ単位を一括して製造することができる。その場合、最後にテープ基材１２１を半導体パッケージ単位に切り分けて個々の半導体装置１０１（図２４）を得ることができる。

【００７０】〔実施例６〕図２６（１）および（２）に、第２発明による半導体装置の他の例を（１）断面図および（２）上面図でそれぞれ示す。本実施例の半導体装置１０２においては、実施例５の導体柱１３２の代わりに、外部接続端子１２８が、金属配線１２５の下面から下方に延びてテープ基材１２１を貫通して下方に突出している。それ以外は実施例５と同じ構造である。外部接続端子１２８の材料は、導体柱１３２に用いるのと同じ材料から選択できる。

【００７１】図２７を参照して、図２６に示した半導体装置１０２の製造方法を説明する。本実施例は、実施例１～４と同様に多数の半導体パッケージ単位について一括して製造する場合に適用できるが、以下においては、説明を簡潔にするために、単一の半導体パッケージ単位について製造する形で説明する。先ず、図２７（１）に示すように、アクティブ面１２３Ａに接続端子１２９を備えた半導体素子１２３と、テープ基材１２１を準備する。テープ基材１２１は、上面に金属配線１２５を備え、外部接続端子１２８に対応する位置に厚さ方向の貫通孔１２１Ｈを有し、金属配線１２５の下面が貫通孔１２１Ｈの上端を塞いで画定している。接続端子１２９の形成方法、テープ基材１２１の材料構成、金属配線１２５の形成方法は、実施例１と同様である。貫通孔１２１Ｈの形成方法は、実施例１の貫通孔２２と同様である。

【００７２】次に、図２７（２）に示したように、実施例５の図２５（２）の工程と同様にして、テープ基材１２１の上面に半導体素子を搭載する。

【００７３】次に、図２７（３）に示したように、実施例５の図２５（４）の工程と同様に封止樹脂層１２４を形成する。

【００７４】次に、図２７（４）に示すように、封止樹脂層１２４の上部および半導体素子１２３の背面側部分を研削および研磨して所定厚さとする。図２７（３）の工程で、封止樹脂層１２４の上面が半導体素子１２３の上面（背面）より高く、半導体素子１２３全体が封止樹脂層１２４の内部に埋め込まれた状態としてあるが、必ずしもその必要はなく、後の研削および研磨により、半導体素子１２３を含めた全体を所定厚さとすることができるように封止樹脂層１２４の厚さを設定すればよい。

【００７５】次に、図２７（５）に示すように、外部接続端子１２８を形成する。外部接続端子１２８は、貫通孔１２１Ｈの上端を画定する金属配線１２５の下面から下方に延びて貫通孔１２１Ｈを充填し下方に突出している。図２７（４）の研削・研磨工程と、図２７（５）の外部接続端子形成工程の順番は、この順でもよいし逆順でもよい。

【００７６】図２７には単一の半導体パッケージ単位についてのみ示したが、実際には複数の半導体素子パッケージ単位を含み得る面積のテープ基材１２１を用いて、図２７（１）～（５）の工程を行うことにより、多数の半導体パッケージ単位を一括して製造することができる。その場合、最後にテープ基材１２１を半導体パッケージ単位に切り分けて個々の半導体装置１０２（図２６）を得ることができる。

【００７７】〔実施例７〕図２８（１）および（２）に、第２発明による半導体装置のもう一つの例を（１）断面図および（２）上面図でそれぞれ示す。本実施例の半導体装置１０３においては、実施例５の導体柱１３２と実施例６の外部接続端子１２８を共に設けてある。本実施例の半導体装置１０３を製造する方法は、実施例５の製造工程と実施例６の製造工程とを組み合わせた方法である。図２５および図２７を参照して、図２８に示した半導体装置１０３の製造方法を説明する。図２８に示した半導体装置１０３は複数層積層して用いることができる。

【００７８】先ず、実施例６と同様に、図２７（１）に示す半導体素子１２３とテープ基材１２１を準備し、図２７（２）に示すようにテープ基材１２１の上面に半導体素子を搭載する。

【００７９】次に、図２５（３）に示すように金属配線１２５の上面に下端が接合した導体柱１３２を形成し、図２５（４）に示すように封止樹脂層１２４を形成する。その後、図２７（４）の研削・研磨工程と図２７（５）の外部接続端子形成工程とをこの順または逆順で行うことにより、図２８の半導体装置１０３が得られる。

【００８０】ここでは単一の半導体パッケージ単位について説明したが、実際には複数の半導体素子パッケージ単位を含み得る面積のテープ基材１２１を用いて、上記の工程を行うことにより、多数の半導体パッケージ単位を一括して製造することができる。その場合、最後にテープ基材１２１を半導体パッケージ単位に切り分けて個々の半導体装置１０３（図２８）を得ることができる。

【００８１】以上で説明した第１発明および第２発明による半導体装置はテープ基材を含む構造である。以下に、テープ基材を含まない構造の第３発明による半導体装置の実施例を説明する。

〔実施例８〕図２９（１）および（２）に、第３発明による半導体装置の一例を断面図で示す。図２９（１）に

示した半導体装置１０４は、所定厚さの樹脂体１２４の内部に半導体素子１２３が封止されており、半導体素子１２３は背面１２３Ｂを樹脂体１２４の上面に露出し、アクティブ面１２３Ａを下方に向けている。樹脂体１２４の下面には金属配線１２５が形成されており、半導体素子１２３のアクティブ面１２３Ａから下方に延びた接続端子１２９が金属配線１２５の上面に接続している。樹脂体１２４の上面と半導体素子１２３の背面１２３Ｂは同一平面を成している。接続端子１２９は、金のスタッドバンプ、めっきバンプ等として形成できる。

【００８２】図２９（２）に示した半導体装置１０４'は、図２９（１）の半導体装置１０４の構造において、金属配線１２５を含めて樹脂体１２４の下面をソルダレジスト層１２６が覆っており、金属配線１２５の下面に形成された接続バンプ１２８がソルダレジスト層１２６を貫通して下方に突き出ている。

【００８３】図３０を参照して、図２９に示した半導体装置１０４および１０４'の製造方法を説明する。本実施例は、実施例１～４と同様に多数の半導体パッケージ単位について一括して製造する場合に適用できるが、以下においては、説明を簡潔にするために、単一の半導体パッケージ単位について製造する形で説明する。先ず、図３０（１）に示すように、半導体素子１２３のアクティブ面１２３Ａに形成された接続端子１２９の先端を、超音波接合や、インジウム等の低融点金属を介した合金接合などの方法により、Ａｌ箔、Ｃｕ箔、金めっきで配線を形成した銅箔、Ｃｕ張りＡｌ箔などの金属基板１２５Ｍの上面に接合することにより、半導体素子１２３を金属基板１２５Ｍ上に搭載する。

【００８４】次に、図３０（２）に示すように、金属基板１２５Ｍの上面全体を樹脂で覆うことにより、樹脂体１２４を形成する。樹脂体１２４は内部に半導体素子１２３を封止しており、下面が金属基板１２５Ｍと接合している。樹脂体１２４としては、エポキシ樹脂、ポリイミド樹脂、シアノエステル樹脂、多環芳香族系樹脂を用いることができ、特にエポキシ樹脂が望ましい。樹脂体１２４の熱膨張係数および熱伝導率を調整するために、無機フィラーとして、シリカ、アルミナ、窒化アルミニウム等のセラミック粒子を分散させることができる。分散量は、所望の熱膨張係数および熱伝導率の値に応じて設定する。粒径は２～１０μｍ で粒子形状は球状に近いほど望ましい。

【００８５】次に、図３０（３）に示すように、金属基板１２５Ｍをパターニングすることにより、樹脂体１２４の下面に金属配線１２５を形成する。金属配線１２５は上面が接続端子１２９に接続している。次に、樹脂体１２４の上部および半導体素子１２３の背面側部分を研削および研磨して所定厚さとする。以上の工程により、図２９（１）に示した半導体装置１０４が完成する。

【００８６】更に、図３０（３）の工程の次に、図３０（４）に示すように、金属配線１２５を含めて樹脂体１２４の下面全体を覆うソルダレジスト層１２６を形成し、ソルダレジスト層１２６に貫通孔１２７を形成する。貫通孔１２７は下端が開口し、上端が金属配線１２５の下面により塞がれて画定されている。

【００８７】次に、図３０（５）に示したように、樹脂体１２４の上部および半導体素子１２３の背面側部分を研削および研磨して所定厚さとする。

【００８８】次に、図３０（６）に示すように、貫通孔１２７を充填して下方に突き出た外部接続端子１２８を形成する。これは、図２５（３）に示した導体柱１３２と同様に、はんだボールの搭載か、はんだペースト印刷後リフローすることにより行う。なお、図３０（５）の研削・研磨工程と図３０（６）の外部接続端子形成工程とは逆順に行ってもよい。これにより、図２９（２）に示した半導体装置１０４'が完成する。

【００８９】ここでは単一の半導体パッケージ単位について説明したが、実際には複数の半導体素子パッケージ単位を含み得る面積の金属基板１２５Ｍを用いて、上記の工程を行うことにより、多数の半導体パッケージ単位を一括して製造することができる。その場合、最後に金属基板１２５Ｍを半導体パッケージ単位に切り分けて個々の半導体装置１０４あるいは１０４'（図２９）を得ることができる。

【００９０】次に図３１を参照して、図２９に示した半導体装置１０４および１０４'の、他の製造方法を説明する。先ず、図３１（１）に示すように、金属基板１２５Ｍの上面に異種金属の配線パターン１２５を設けた複合金属板１２５Ａを作製する。これは、Ｃｕ箔から成るＣｕ基板１２５Ｍ上にＡｕめっきによりＡｕ配線パターン１２５を設けるか、または、Ｃｕ張りＡｌ箔のＣｕをエッチングしてパターニングすることによりＡｌ基板１２５Ｍ上にＣｕ配線パターン１２５を設けることにより行う。

【００９１】次に、図３１（２）に示すように、半導体素子１２３のアクティブ面１２３Ａに形成された接続端子１２９の先端を、超音波接合やインジウム等の低融点金属を介した合金接合などの方法により、配線パターン１２５の上面に接合することにより、半導体素子１２３を複合金属板１２５Ａ上に搭載する。

【００９２】次に、図３１（３）に示すように、配線パターン１２５を含めて複合金属板１２５Ａの上面全体を樹脂で覆うことにより、樹脂体１２４を形成する。樹脂体１２４は内部に半導体素子１２３を封止しており、下面が配線パターン１２５および金属基板１２５Ｍと接合している。樹脂体１２４は、図３０（２）について説明したものと同様の材質である。

【００９３】次に、図３１（４）に示すように、エッチングにより金属基板１２５Ｍを除去する。具体的には、Ａｕ配線パターン１２５／Ｃｕ箔基板１２５Ｍの組み合

わせの場合には、Ｃｕは溶解するがＡｕは溶解しないエッチャントを用いたエッチングによりＣｕ箔基板１２５Ｍを除去する。あるいは、Ｃｕ配線パターン１２５／Ａｌ基板１２５Ｍの組み合わせの場合には、Ａｌは溶解するがＣｕは溶解しないエッチャントを用いたエッチングによりＡｌ基板１２５Ｍを除去する。これにより、樹脂体１２４の下面にＡｕまたはＣｕから成る金属配線１２５が接合された構造が得られる。次に、樹脂体１２４の上部および半導体素子１２３の背面側部分を研削および研磨して所定厚さとする。以上の工程により、図２９（１）に示した半導体装置１０４が完成する。ただし樹脂体１２４とソルダレジスト層１２６との接合面の位置は、図２９（１）の構造では金属配線１２５の上面と同一面となるが、上記工程で得られた得られた構造では金属配線１２５の下面と同一面となる点で異なる。

【００９４】更に、図３１（４）の工程の次に、図３１（５）、（６）、（７）に示す順序で、ソルダレジスト層１２６の形成、研削・研磨、外部接続端子１２８の形成を、それぞれ図３０（４）、（５）、（６）に示した工程と同様の手順で行う。この場合にも、図３１（６）の研削・研磨工程と図３１（７）の外部接続端子形成工程とは逆順に行ってもよい。これにより図２９（２）に示した半導体装置１０４’が完成する。ただし樹脂体１２４とソルダレジスト層１２６との接合面の位置は、図２９（２）の構造では金属配線１２５の上面と同一面となるが、上記工程で得られた得られた構造では金属配線１２５の下面と同一面となる点で異なる。

【００９５】〔実施例９〕図３２に、第３発明による半導体装置の他の例を断面図で示す。図３２（１）、（２）、（３）にそれぞれ示した半導体装置１０５、１０５’、１０５”はいずれも、図２９（１）に示した半導体装置１０４の構造に加えて、複数の導体柱１３２を更に備えている。導体柱１３２は、金属配線１２５の上面から樹脂体１２４を貫通して上方に延びており、上端が樹脂体１２４の上面に露出している。ここで、図３２（１）の半導体装置１０５は導体柱１３２の上端のみが樹脂体１２４から露出しており、図３２（２）の半導体装置１０５’は導体柱１３２の上端および側面が樹脂体１２４から露出している。

【００９６】図３２（３）の半導体装置１０５”は、上端のみが樹脂体１２４から露出している導体柱１３２Ａと、上端および側面が樹脂体１２４から露出している導体柱１３２Ｂとを備えており、金属配線１２５を含めて樹脂体１２４の下面を覆うソルダレジスト層１２６が形成されている。ただし、ソルダレジスト層１２６は、側面が露出した導体柱１３２Ｂと接続している金属配線１２５の部分は覆っておらず、この部分で金属配線１２５の下面は露出している。導体柱１３２、１３２Ａ、１３２Ｂは、銅（Ｃｕ）、ニッケル（Ｎｉ）、コバール（商品名）等の金属または合金、あるいは錫－銀（Ｓｎ－Ａｇ）合金、錫－鉛（Ｓｎ－Ｐｂ）合金等の低融点合金で形成することができる。

【００９７】図３２に示した半導体装置１０５、１０５’、１０５”を製造するには、実施例８において図３０により説明した製造工程に用いる金属基板１２５Ｍの上面に、予めスタッドバンプ形成、金属柱の接合等により導体柱１３２を形成しておき、実施例８と同様に図３０の工程を適宜行えばよい。

【００９８】〔実施例１０〕図３３に、図３２（１）に示した半導体装置１０５を複数層積層した素子積層型半導体装置の例を示す。図示した半導体装置１０６は、半導体装置１０５を３層積層したものであり、図３２（１）の構造に加えて図２９（２）と同様にソルダレジスト層１２６と接続バンプ１２８とを形成した後、積層して一体としたものである。下層の導体柱１３２の上端と、上層の金属配線１２５の下面とが、接続バンプ１２８を介して相互に電気的に接続している。

【００９９】〔実施例１１〕図３４（１）に、図３２（２）に示した半導体装置１０５’を側面で相互に接続した素子並列型半導体装置の例を示す。図示した半導体装置１０７は、２個の半導体装置１０５’を並列に接続したものであり、側端部を除き金属配線１２５を含めて樹脂体１２４の下面をソルダレジスト層１２６で覆い、樹脂体１２４の側面に露出した導体柱１３２の側面同士ではんだ等の低融点金属１３８を介して相互に電気的に接続されている。この接続は下記のように行うことができる。低融点金属ボールを搭載した後、または低融点金属ペーストの印刷またはドッティングにより低融点金属を供給した後、リフローすることにより、低融点金属１３８が金属配線１２５および導体柱１３２の露出面に広がり、接合が行われる。接合部の間隔が広い場合は導体ペーストのドッティングによって接合することもできる。

【０１００】図３４（２）に、図３２（２）に示した半導体装置１０５’を積層し且つ並列接続した素子積層並列型半導体装置の例を示す。図示した半導体装置１０８は、２個の半導体装置１０５’を並列に接続した層が２層積層されて成る。各半導体装置１０５’同士の接続関係は、図３３の素子積層型半導体装置１０６と図３４（１）の素子並列型半導体装置１０７とを組み合わせた関係である。

【０１０１】〔実施例１２〕図３５（１）に、キャパシタを含む第３発明の半導体装置の例を示す。図示した半導体装置１０９は、図２９（２）の半導体装置１０４’の構造に加えて、樹脂体１２４中に封止されたキャパシタ１４３を備えている。キャパシタ１４３は両極の電極端子１４５が金属配線１２５の上面に直接接続されている。図３５（２）に示したように、望ましくはキャパシタ１４３は対向平板型であり、各導体パターン１４７のパターン面が樹脂体１２４の厚さ方向に平行である。キ

ャパシタ１４３は例えば通常のセラミック積層型コンデンサであり、導体パターン１４７間はチタン酸ストロンチウムのような誘電体１４９で充填されている。静電容量すなわち有効面積が、研削・研磨後の厚さによって決まるため、最終厚さを見込んで設計する必要がある。

【０１０２】キャパシタ１４３としては、市販のチップキャパシタ（チップコンデンサ）が好適に用いられる。なお、キャパシタ１４３を含む構造は、図３５（１）に示す半導体装置に限らず、図２４、図２９（１）、図３２に示す半導体装置にも適用できる。

【０１０３】

【発明の効果】本発明によれば、取り付け高さを低減すると同時に均一化し、個々のチップ取り付けのための煩雑な工程を必要とせず、製造歩留りを向上し、チップの厚さばらつきに影響されずに半導体装置の高さを均一化し、電気試験の一括実行が可能な薄型半導体パッケージとしての半導体装置およびその製造方法が提供される。

【図面の簡単な説明】

【図１】図１は、半導体チップとＴＣＰのリードを接続した後の従来の半導体装置を示す斜視図であり、個々のＴＣＰをテープから切断する前の状態を示す。

【図２】図２は、従来の半導体チップとパッケージのリードの接続の状態を、図１の半導体装置の中心部を拡大して示す断面図である。

【図３】図３（１）および（２）は、第１発明による半導体装置の一例を示すそれぞれ（１）断面図および（２）上面図である。

【図４】図４は、図３に示した第１発明の半導体装置を製造するために最初に準備する初期構造を示す断面図である。

【図５】図５は、図４に示した初期構造に絶縁性コーティングを形成した状態を示す断面図である。

【図６】図６は、硬化前のコーティングの上に半導体素子を配置して接合する工程を示す断面図である。

【図７】図７は、半導体素子が搭載された領域以外のテープ基材の上面を覆い且つ少なくとも半導体素子の側面周囲を封止する封止樹脂層を形成した状態を示す断面図である。

【図８】図８は、図７とは別の態様により、半導体素子が搭載された領域以外のテープ基材の上面を覆い且つ少なくとも半導体素子の側面周囲を封止する封止樹脂層を形成した状態を示す断面図である。

【図９】図９は、封止樹脂層の上部および半導体素子の背面側部分を研削および研磨して所定の厚さとし、外部接続端子を形成した状態を示す断面図である。

【図１０】図１０（１）および（２）は、第１発明による半導体装置の他の例を示すそれぞれ（１）断面図および（２）上面図である。

【図１１】図１１は、図１０の半導体装置を複数層積層して形成した薄型の積層型半導体装置を示す断面図である。

【図１２】図１２は、図１０に示した第１発明の半導体装置を製造するために最初に準備する初期構造を示す断面図である。

【図１３】図１３は、図１２に示した初期構造に低融点金属の導体および絶縁性コーティングを形成した状態を示す断面図である。

【図１４】図１４は、硬化前のコーティングの上に半導体素子を配置して接合する工程を示す断面図である。

【図１５】図１５は、半導体素子が搭載された領域以外のテープ基材の上面を覆い且つ少なくとも半導体素子の側面周囲を封止する封止樹脂層を形成した状態を示す断面図である。

【図１６】図１６は、封止樹脂層の上部および半導体素子の背面側部分を研削および研磨して所定の厚さとし、外部接続端子を形成した状態を示す断面図である。

【図１７】図１７（１）および（２）は、第１発明による半導体装置のもう一つの例をそれぞれ示す（１）断面図および（２）上面図である。

【図１８】図１８は、図１７の半導体装置を複数層積層して形成した薄型の積層型半導体装置を示す断面図である。

【図１９】図１９は、図１７に示した第１発明の半導体装置を製造するために最初に準備する初期構造を示す断面図である。

【図２０】図２０は、図１９に示した初期構造に絶縁性コーティングを形成し、硬化前のコーティングの上に半導体素子を配置して接合する工程を示す断面図である。

【図２１】図２１は、半導体素子と絶縁性基材の開口との間隙を封止樹脂層で封止した状態を示す断面図である。

【図２２】図２２は、図２１に示す状態から、絶縁性基材の上部、封止樹脂層の上部および半導体素子の背面側部分を研削および研磨して所定の厚さとし、外部接続端子を形成した状態を示す断面図である。

【図２３】図２３は、テープ基材を含む初期構造として、ディスク状のものを用いて製造した切り分けまえの構造を一部断面で示す斜視図である。

【図２４】図２４（１）、（２）および（３）は、第２発明による半導体装置の一例を示す（１）断面図、（２）断面図および（３）上面図である。

【図２５】図２５は、図２４（１）の半導体装置を製造するための工程を示す断面図である。

【図２６】図２６（１）および（２）は、第２発明による半導体装置の他の例を示す（１）断面図および（２）上面図である。

【図２７】図２７は、図２６の半導体装置を製造するための工程を示す断面図である。

【図２８】図２８（１）および（２）は、第２発明による半導体装置のもう一つの例を示す（１）断面図および

（２）上面図である。

【図２９】図２９（１）および（２）は、第３発明による半導体装置の一例を示す断面図である。

【図３０】図３０は、図２９の半導体装置を製造するための工程の一例を示す断面図である。

【図３１】図３１は、図２９の半導体装置を製造するための工程の他の例を示す断面図である。

【図３２】図３２（１）、（２）および（３）は、第３発明による半導体装置の他の例を示す断面図である。

【図３３】図３３は、図３２の半導体装置を複数層積層して形成した薄型の積層型半導体装置を示す断面図である。

【図３４】図３４（１）および（２）は、図３２の半導体装置を（１）並列接続した素子並列型半導体装置および（２）積層かつ並列接続した素子積層並列型半導体装置をそれぞれ示す断面図である。

【図３５】図３５は、キャパシタを含む第３発明の半導体装置の例を示す（１）断面図および（２）部分拡大断面図である。

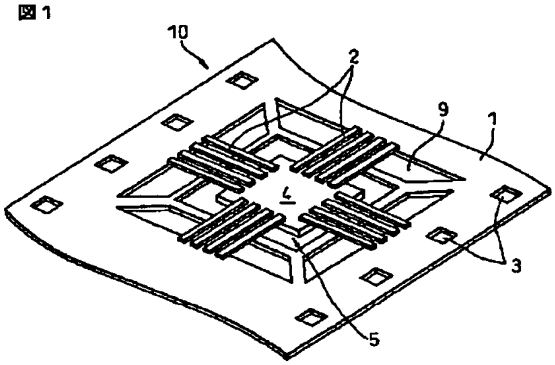
【符号の説明】

１…樹脂フィルム（基材）
２…リード
３…スプロケットホール
４…半導体チップ（半導体素子）
５…開口（デバイスホール）
６…バンプ（金等）
７…封止樹脂
１０…従来のＴＣＰ
２０…第１発明による半導体装置
２１…絶縁性テープ基材
２２…テープ基材２１の厚さ方向の貫通孔
２３…半導体素子
２３Ａ…半導体素子のアクティブ面
２３Ｂ…半導体素子の背面
２４…封止樹脂層
２５…金属配線
２６…ソルダレジスト層
２７…ソルダレジスト層の厚さ方向の貫通孔
２８…外部接続端子
２９…半導体素子の接続端子
３０…低融点金属の充填材

３１…絶縁性のコーティング
３２…低融点金属の導体（柱状導体）
３６…絶縁性基材
３７…絶縁性基材３６の厚さ方向の貫通孔
４０…第１発明による半導体装置
４４…第１発明による素子積層型半導体装置
６０…第１発明による半導体装置
６６…第１発明による素子積層型半導体装置
１０１…第２発明による半導体装置
１０２…第２発明による半導体装置
１０３…第２発明による半導体装置
１０４…第３発明による半導体装置
１０４’…第３発明による半導体装置
１０５…第３発明による半導体装置
１０５’…第３発明による半導体装置
１０５”…第３発明による半導体装置
１０６…第３発明による素子積層型半導体装置
１０７…第３発明による素子並列型半導体装置
１０８…第３発明による素子積層並列型半導体装置
１０９…第３発明によるキャパシタを備えた半導体装置
１２１…絶縁性テープ基材
１２１Ｈ…絶縁性テープ基材の貫通孔
１２３…半導体素子
１２３Ａ…半導体素子のアクティブ面
１２３Ｂ…半導体素子の背面
１２４…封止樹脂層
１２５…金属配線（配線パターン）
１２５Ａ…複合金属板
１２５Ｍ…金属基板
１２６…ソルダレジスト層
１２７…ソルダレジスト層の貫通孔
１２８…外部接続端子または接続バンプ
１２９…半導体素子の接続端子
１３２…導体柱
１３２Ａ…導体柱
１３２Ｂ…導体柱
１４３…キャパシタ
１４５…キャパシタの電極端子
１４７…キャパシタの対向する平板
１４９…キャパシタの平板間を満たす誘電体

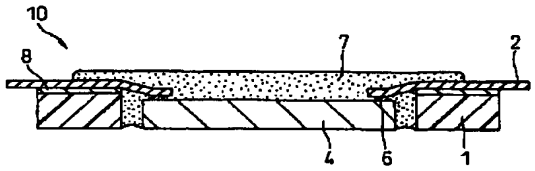
【図１】

図１



【図２】

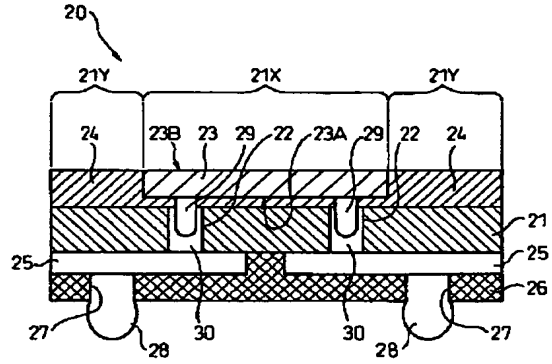
図２



【図３】

図３

(1)



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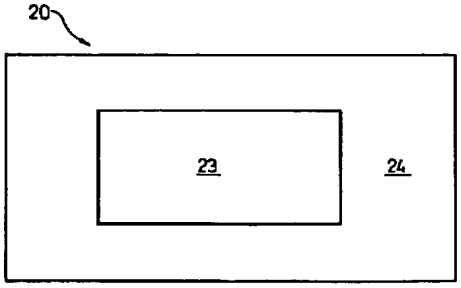

【図１０】

図１０

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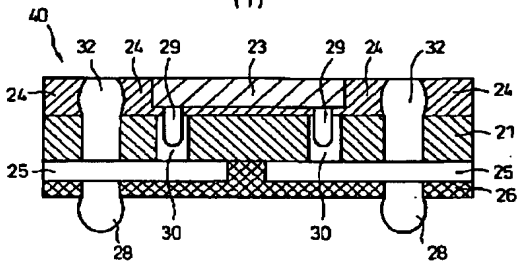

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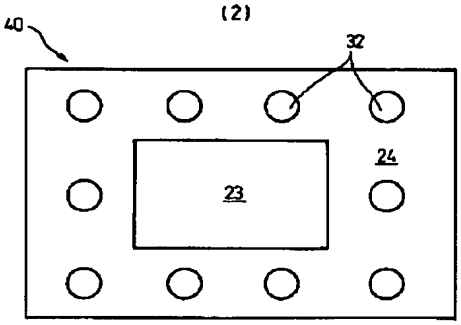

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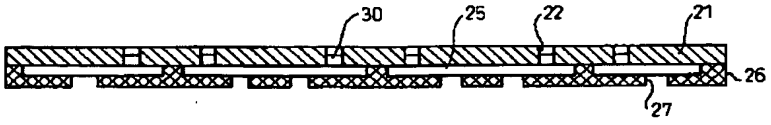

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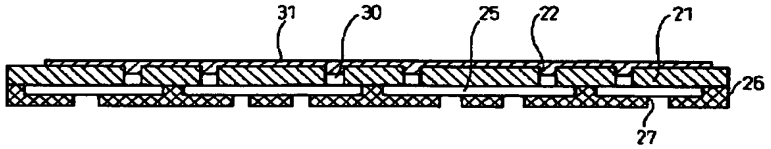

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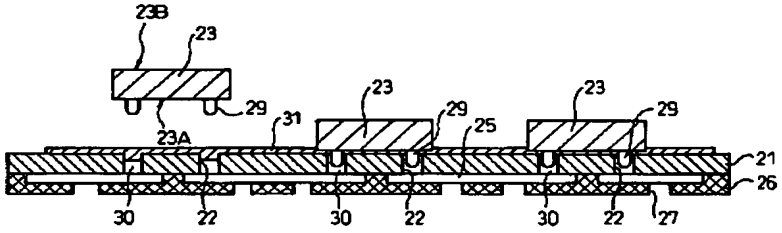

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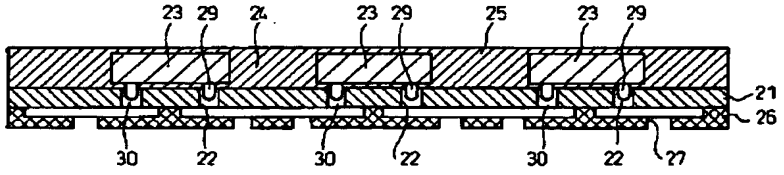

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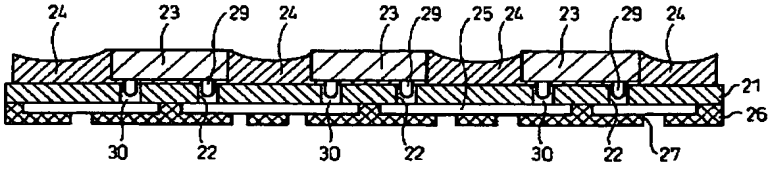

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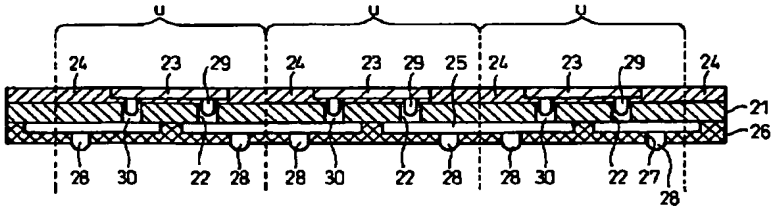

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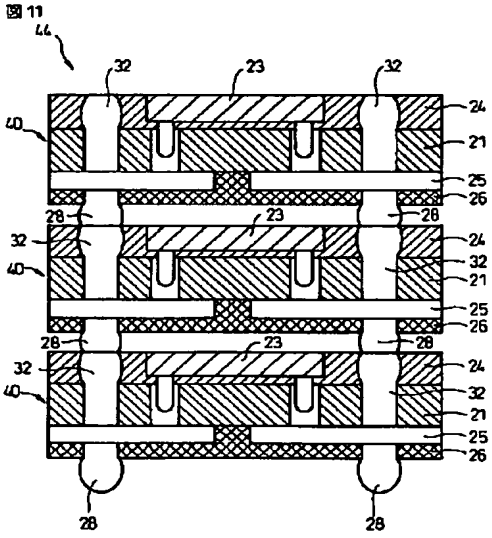

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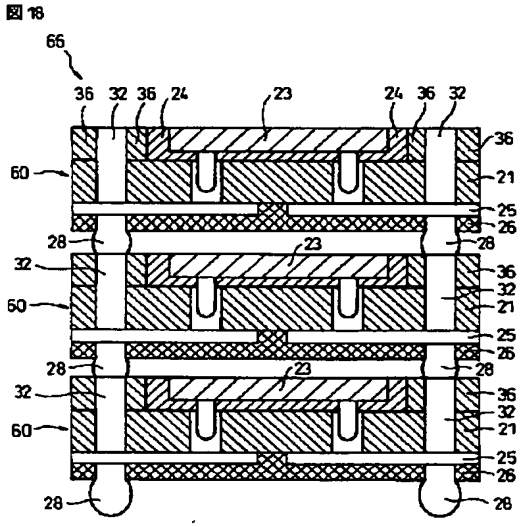

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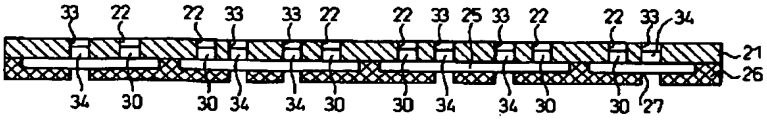

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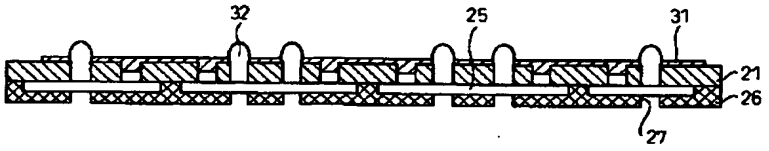

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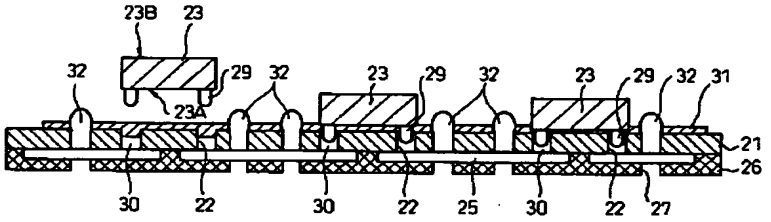

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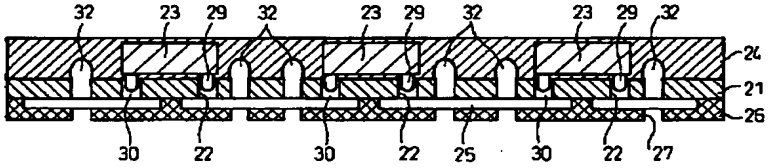

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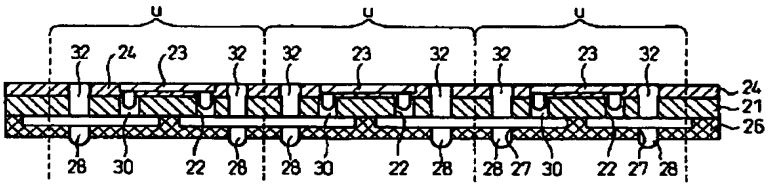

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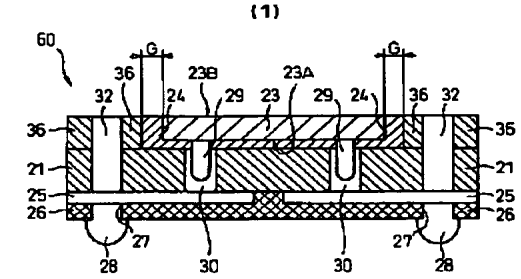

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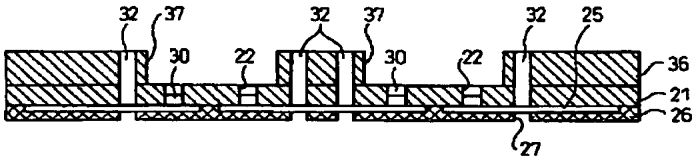

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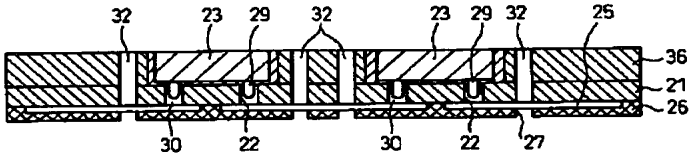

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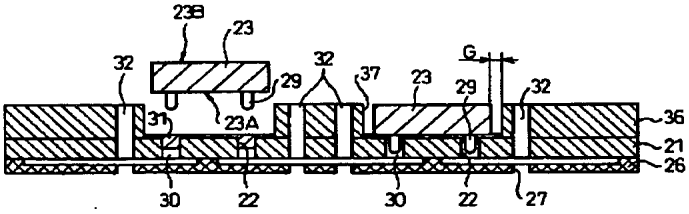

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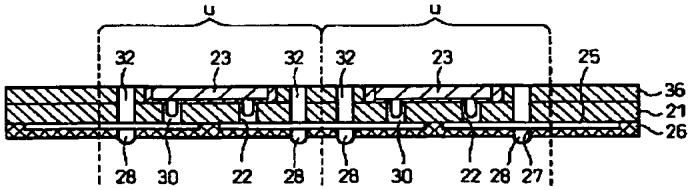

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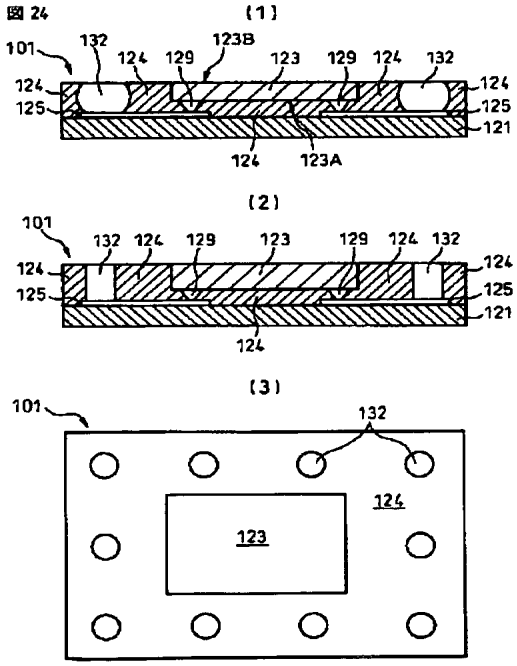

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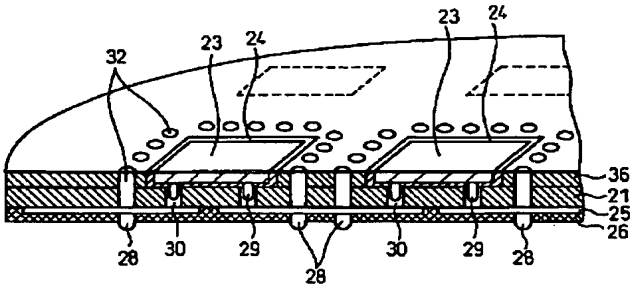

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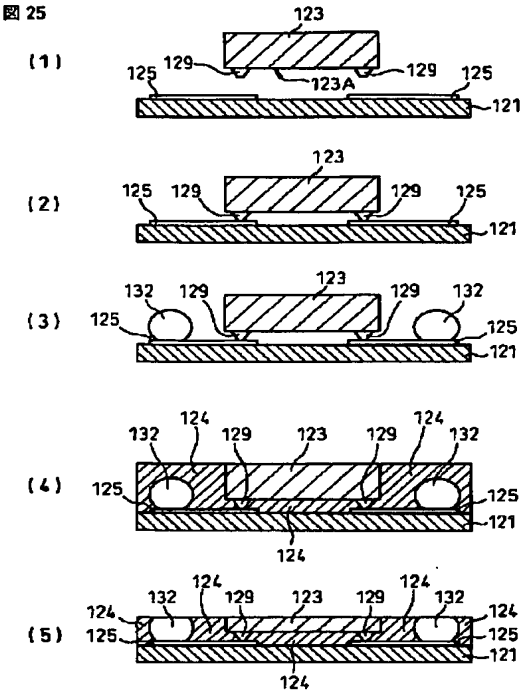

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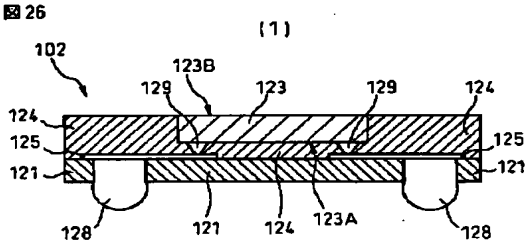

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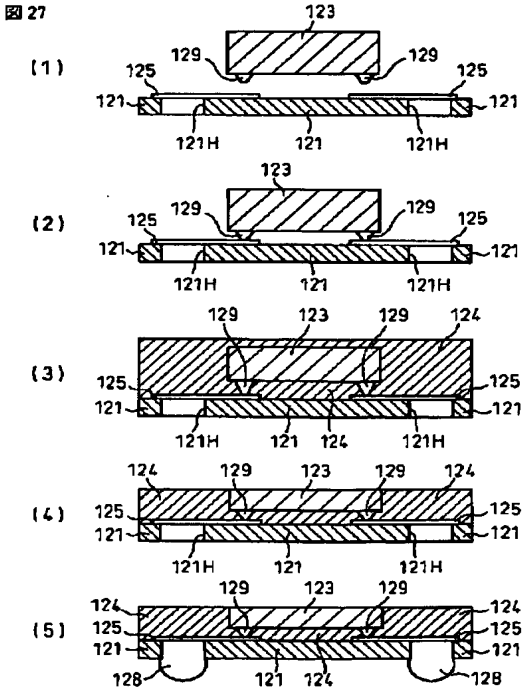

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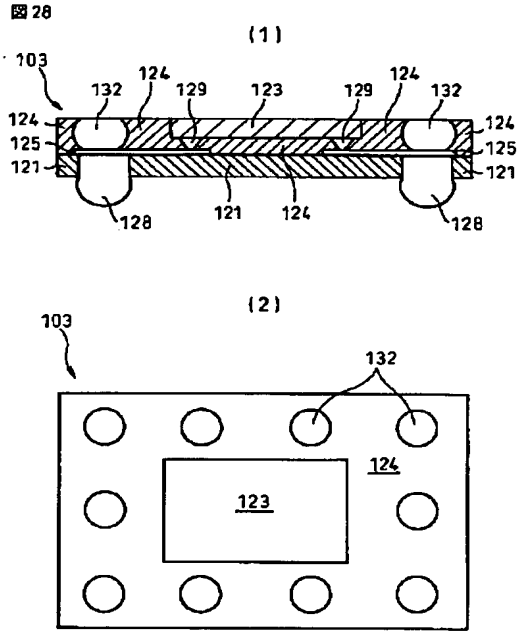

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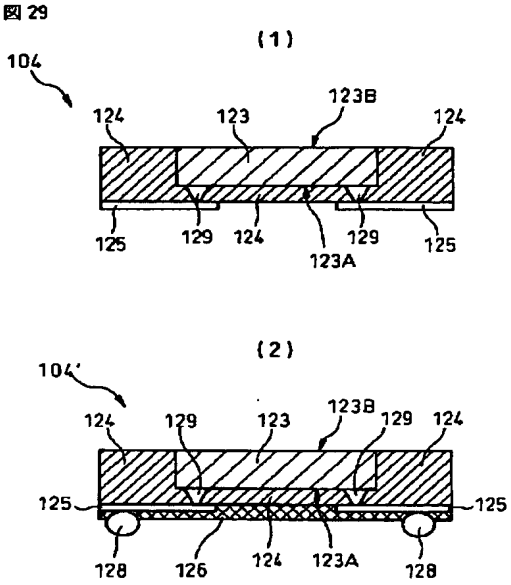

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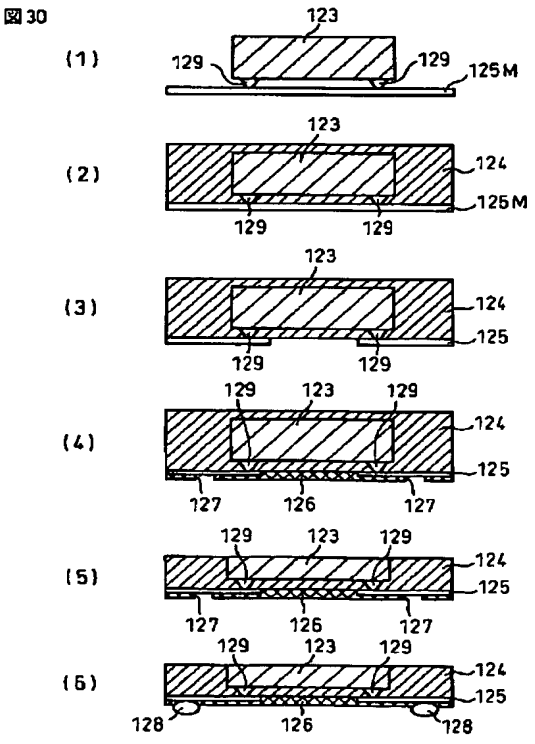

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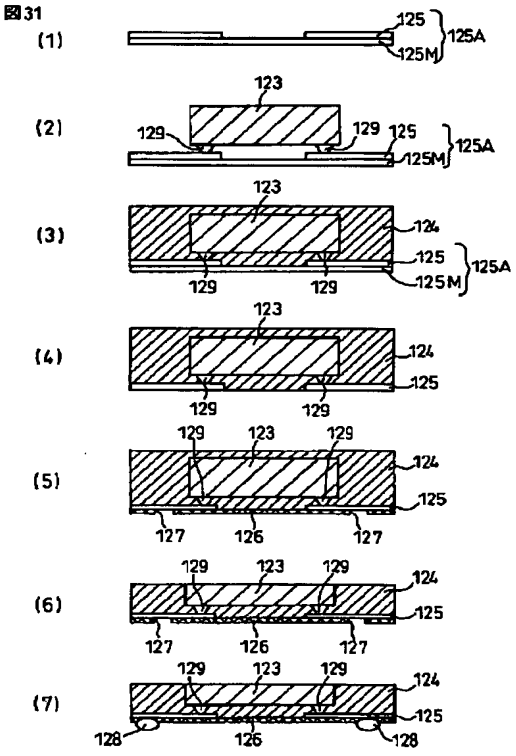

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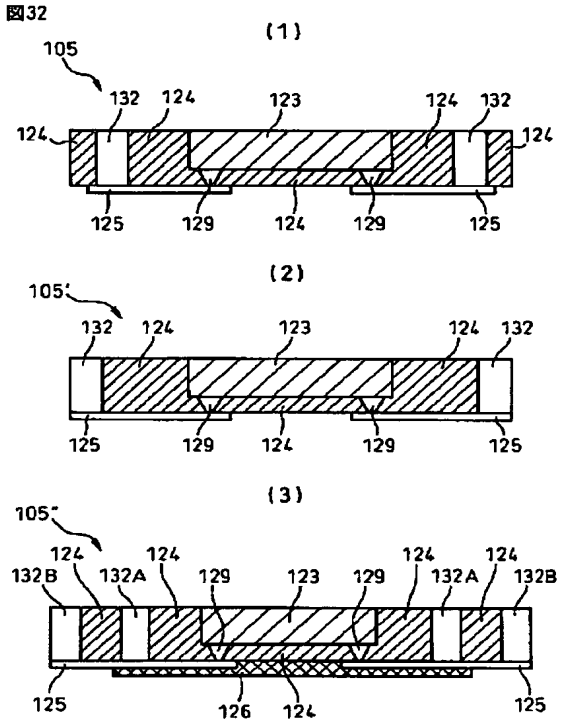
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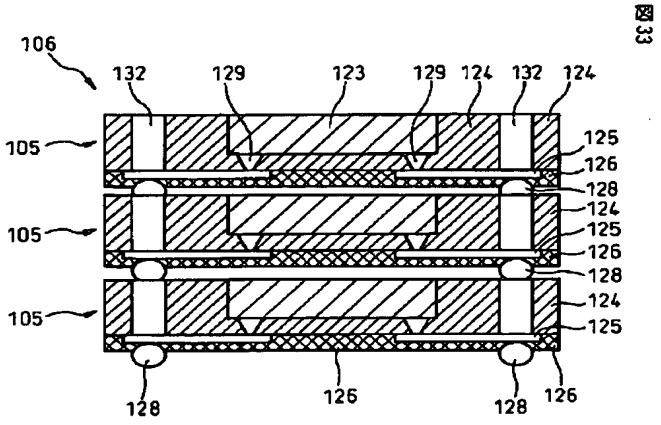
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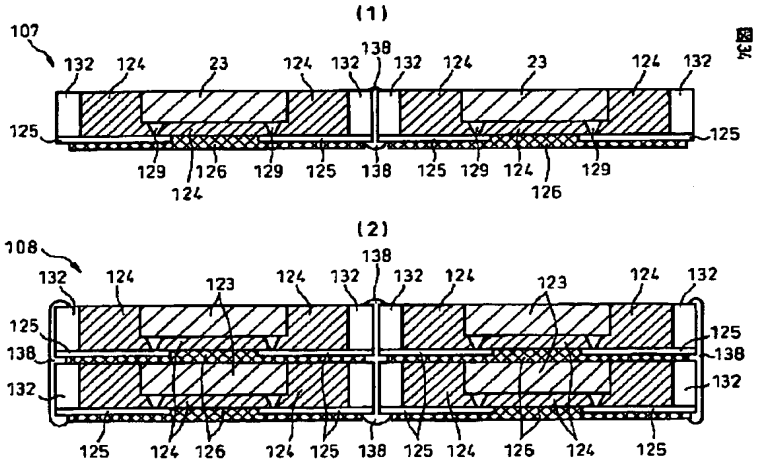
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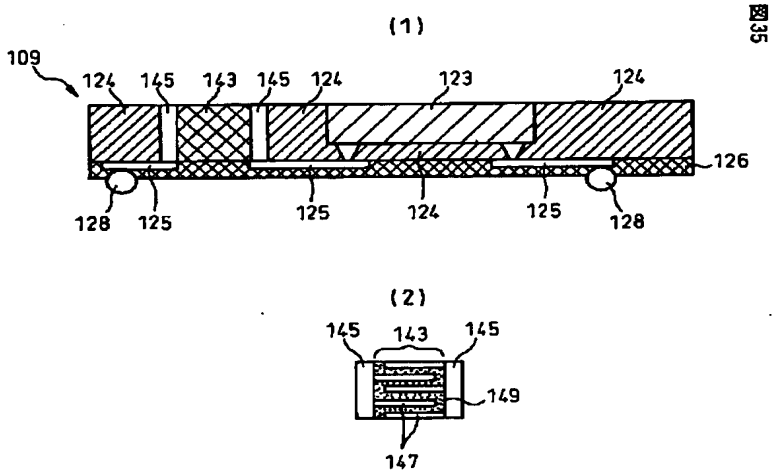

フロントページの続き

(51) Int. Cl.[7]	識別記号	F I	ﾃｰﾏｺｰﾄﾞ(参考)
H01L 25/18			

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